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IDA PAPER P-1600

BUILT-IN-TEST EQUIPMENT REQUIREMENTS WORKSHOP

Workshop Presentation

August 1981

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Prepared for
Assistant Secretary of Defense Manpower Reserve Affairs and Logistics

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM	
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER	
	DD-A 107 842		
4. TITLE (and Subtitle)		5. TYPE OF REPORT & PERIOD COVERED	
BUILT-IN-TEST EQUIPMENT REQUIREMENTS WORKSHOP		Final	
		6. PERFORMING ORG. REPORT NUMBER	
		Paper P-1600	
7. AUTHOR(s)		8. CONTRACT OR GRANT NUMBER(s)	
Workshop Presentation		MDA903 79 C 0320	
9. PERFORMING ORGANIZATION NAME AND ADDRESS		10. PROGRAM ELEMENT PROJECT TASK AREA & WORK UNIT NUMBERS	
Institute for Defense Analyses Program Analysis Division 400 Army-Navy Drive Arlington, Virginia 22202		Task 81-1	
11. CONTROLLING OFFICE NAME AND ADDRESS		12. REPORT DATE	
Assistant Secretary of Defense Manpower Reserve Affairs and Logistics The Pentagon Washington, DC 20301		August 1981	
		13. NUMBER OF PAGES	
		219	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report)	
		UNCLASSIFIED	
		15a. DECLASSIFICATION DOWNGRADING SCHEDULE	
		N/A	
13. DISTRIBUTION STATEMENT (of this Report)			
Approved for public release; distribution unlimited.			
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)			
18. SUPPLEMENTARY NOTES			
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)			
Built-in-Test (BIT), 100 Percent Diagnostics, diagnostic specification, fault detection, troubleshooting, performance levels, safety, mission critical functions, false alarm rate, operational tests, Self-Test (ST), System BIT, Subsystem BIT			
20. ABSTRACT (Continue on reverse side if necessary and identify by block number)			
A workshop was held for the purpose of assessing progress and problems in specifying and testing Built-in-Test (BIT) used in complex electronic equipment. The workshop's principal recommendation is that the current specification and test approach be broadened to include all capabilities associated with the detection and isolation of faults. Current practices generally address only a narrow subset of these capabilities, namely, BIT. The workshop participants defined this broad capability (continued)			

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(Item 20, continued)
as "100 Percent Diagnostics." The diagnostic capability is considered to have two components--"automatic" and "manual." The automatic component consists of BIT or semi-automatic BIT with technical manuals, while the manual component consists of personnel using logic, external test equipment and/or manual test procedures. Observations on current experience with BIT, recommendations to improve specification and testing of "100 Percent Diagnostics" that can be put into practice in the near term, and proposed research areas are presented.

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BUILT-IN-TEST EQUIPMENT
REQUIREMENTS WORKSHOP

Workshop Presentation

August 1981



INSTITUTE FOR DEFENSE ANALYSES
PROGRAM ANALYSIS DIVISION
400 Army-Navy Drive, Arlington, Virginia 22202

Contract MDA 903 79 C 0320
Task 81-1

i/ii

PREFACE

This paper was prepared by the Institute for Defense Analyses (IDA) for the Office of the Assistant Secretary of Defense (OASD), Manpower, Reserve Affairs and Logistics (MRA&L), under Contract MDA903 79 C 0320, Task Order 81-1.

The purpose of the paper (and the workshop which it reports on) was threefold: to assess the state of the art in built-in-test (BIT) equipment with particular emphasis on specification, testing and evaluation; to develop guidelines for specifying requirements for BIT and for its test and evaluation; and to identify areas for research in BIT specification, development and mechanization.

The task commenced on 1 October 1980 and concluded on 28 February 1981; draft publication of the workshop results was scheduled for 28 February 1981, and final publication for 30 April 1981. This publication is issued in fulfillment of the contract.

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EXECUTIVE SUMMARY

The Office of the Secretary of Defense (MRA&L) sponsored a workshop to assess progress and problems in specifying and testing Built-In-Test (BIT) used in complex electronic equipment. The workshop's principal recommendation is that the current specification and test approach be broadened to include all capabilities associated with the detection and isolation of faults. Current practices generally address only a narrow subset of these capabilities, that is, BIT. The workshop participants defined this broad capability as "100 Percent Diagnostics."¹ The diagnostic capability is considered to have two components--"automatic" and "manual." The automatic component consists of BIT or semi-automatic BIT with technical manuals, while the manual component consists of personnel using logic, external test equipment and/or manual test procedures. Observations on current experience with BIT, recommendations to improve specification and testing of "100 Percent Diagnostics" that can be put into practice in the near term, and proposed research areas are discussed below.

The workshop, with both industry and the Services represented, was organized around a case study/discussion format. Presentations were selected to illustrate successful examples of BIT specification, test and evaluation and to represent a wide range of applications. These case studies were presented to individuals with experience in specification, design, test

¹This terminology was used by workshop participants and will be used throughout the workshop proceedings. There is no accepted "standard" terminology in this area.

and evaluation of BIT. Workshop recommendations were presented on the final day to senior Service and Office of the Secretary of Defense managers.

A. OBSERVATIONS

The following summarizes those observations on the performance of systems with BIT which were consistently made by the various participants during workshop discussions.

- BIT-equipped weapon system electronic subsystems (and equipment) being introduced into the field today are not meeting the diagnostic specifications which are generally in the range of 90 to 95 percent probability of *automatic* (or semi-automatic) fault detection and isolation. In addition, experience shows that 20 to 40 percent of the items which were replaced because of a failure indication by BIT are later found to have no failure (principally based on data from both military and civilian aircraft maintenance experience). The unnecessary removal rates are not often part of this specification.
- Even where BIT specifications are close to being met, the systems have been found difficult to maintain, as indicated by long troubleshooting times.
- BIT, in general, is not designed to detect all failure conditions (such as out-of-tolerance conditions or simultaneous failures). Consequently, *manual* troubleshooting is required to augment the automatic (BIT) capability and is particularly needed for the more difficult maintenance problems.
- Manpower planning based on the use of low skilled technicians (i.e., not trained in system operation) for system maintenance combined with BIT capability frequently has to be changed. High skilled technicians who understand system operations in order to correct those discrepancies not solved by low skill level plus BIT combination have had to be included.
- Today's state of the art for mechanization of BIT capability is not advanced to the point where the requirement for highly skilled technicians familiar with troubleshooting can be eliminated.
- There is little visibility to program management during system development of the progress of the BIT design.

- Adequate test time (or test articles) generally has not been set aside to develop BIT in complex systems prior to putting these systems in the field.
- Contractual BIT laboratory demonstration tests (MIL-STD-471) do not provide reliable predictions of BIT performance in the field.
- BIT contractual specification requirements are open to a wide range of interpretations.
- Early assessment (initial operations test and evaluation) of field operational BIT performance is very difficult because of incomplete software and because of the interactions between operational and maintenance personnel, test equipment and technical manuals. Also, standard Service maintenance data reporting systems do not provide sufficient information to evaluate BIT performance or to solve BIT associated problems.
- About two years of field operations, using dedicated technical personnel and closed-loop data systems, has been found necessary to mature the BIT in complex systems. (Contractor participation has been required during this period.)

B. RECOMMENDATIONS

The consensus recommendations developed by the working groups for specifying and testing diagnostics, including BIT, are presented below in the following general order: development of performance specifications, contract requirements, and testing and evaluation.

(1) SPECIFICATIONS FOR DIAGNOSTICS SHOULD BE DEVELOPED TO MEET USER-DEFINED CONSTRAINTS. The equipment user needs to identify constraints in the form of operational and maintenance parameters such as turnaround time, maximum down time, manpower levels, skill levels, and self-sufficiency in deployment.

(2) THE USER OR PROCURING ACTIVITY SHOULD NOT ARBITRARILY SPECIFY A LEVEL OF BIT PERFORMANCE. BIT specifications should evolve from consideration of other diagnostic specification requirements, design, manpower and support constraints as well as an assessment of the state of the art as discussed in the

following recommendation. The BIT specifications should represent the "best" combination of automatic and manual performance to meet the user-defined constraints with available technology.

(3) CONTRACT SPECIFICATIONS FOR DIAGNOSTICS MUST BE INCLUDED IN THE INITIAL DEVELOPMENT CONTRACT SO AS TO BE AN INTEGRAL PART OF EARLY DESIGN EFFORTS. Contract specifications for diagnostics should evolve from both user-defined constraints and the design process. However, based on observations of the performance of current diagnostic systems, it is apparent that many of the contract specifications establish unrealistic performance levels (for example, BIT percentage of faults detected and isolated). But, performance levels for diagnostic performance need not be completely specified in the initial development contract. Performance levels for some of the diagnostic terms (defined in recommendations 6 and 7) will be directly derivable from user-defined constraints and knowledge of existing hardware and maintenance capability. For other diagnostic terms, realistic, achievable levels of performance may not be readily visible at the start of the design process. In this latter case, diagnostic performance levels will have to evolve through the design process and associated comparability studies. Such factors as current levels of BIT performance, current and projected skills of personnel responsible for maintenance and technology capabilities have to be considered in establishing realistic achievable performance levels for the diagnostics. There was no general consensus on the exact process for establishing these performance levels (this area will need additional research). However, it was agreed that all performance requirements should be firmly established as contractual requirements before significant system design efforts are initiated, generally in the full scale development contract.

(4) SERVICES NEED IMMEDIATELY TO DEVELOP DATA BASES DESCRIBING DIAGNOSTIC CAPABILITIES OF CURRENTLY FIELDIED SYSTEMS. These data are needed to support establishing realistic, achievable diagnostic performance levels.

(5) CONTRACT SPECIFICATIONS FOR DIAGNOSTICS TO MEET OPERATIONAL CONSTRAINTS SHOULD BE STATED IN TERMS OF (A) IDENTIFICATION OF SAFETY AND MISSION CRITICAL FUNCTIONS, (B) FALSE ALARM RATE, AND (C) CONSTRAINTS ON THE USE OF TEST EQUIPMENT.

More specifically:

(a) Safety and mission critical functions that need to be continually monitored for failure need to be considered in the design effort.

(b) The false alarm rate, which is defined as percentage of operator reported failure indications that cannot be confirmed by maintenance personnel, needs to be considered both in the design and test approach. The performance level to be achieved need not be established at the start of the development process (see recommendation 3). (There was disagreement among the workshop participants as to whether the rate should be specified at some finite level or zero. This area needs further research.)

(c) Constraints on the use of external test equipment for on-system maintenance need to be considered in the mechanization approach for diagnostics.

(6) CONTRACT SPECIFICATIONS FOR DIAGNOSTICS TO MEET MAINTENANCE CONSTRAINTS SHOULD BE STATED IN TERMS OF (A) "100 PERCENT DIAGNOSTIC CAPABILITY," INCLUDING (B) THE PERCENTAGE OF THIS CAPABILITY THAT WILL BE AUTOMATIC AND MANUAL, AND (C) THE ASSOCIATED SYSTEM REPAIR TIMES SEPARATELY SPECIFIED FOR AUTOMATIC AND MANUAL COMPONENTS. ADDITIONAL TERMS THAT SHOULD BE SPECIFIED ARE (D) UNNECESSARY REMOVAL RATE, AND (E) PERSONNEL SKILLS.

More specifically:

(a) "100 percent diagnostic capability." Specifications should require the contractor to develop and provide a fault detection and fault isolation (FD/FI) capability that addresses all incidents requiring a maintenance action. This would include all types of incidents requiring maintenance personnel intervention including correction of failures (i.e., material failures or out of tolerance conditions, and/or verification that no failure had occurred). In addition, the 100 percent diagnostic capability applies to all items that make up a system (i.e., black boxes, wiring).

(b) The diagnostic capability should be expressed in terms of the percentages of the capability that will be satisfied automatically (BIT) and manually. However, the specific percentages of automatic and manual diagnosis to be achieved should not be established arbitrarily (recommendation 2) and may be established after the start of the development process (recommendation 3).

(c) System repair times separately specified for automatic and manual components of the diagnostic capability. These times may be expressed either (individually or in combination) as mean repair times, maximum allowable repair times, or a repair time distribution.

(d) Unnecessary removal rate. This was defined as the percentage of units removed from the system that are found not to contain a failure at higher levels of maintenance. The specific rate to be achieved could be established after the start of the development process (recommendation 3).

(e) Personnel skills. There is a need to go as far as possible in specifying skill levels in contracts. Suggested approaches are to specify the percentage of tasks to be performed by high skilled and low skilled personnel or the repair

times associated with specific maintenance actions for each skill level.

(7) CONTRACTS SHOULD INCLUDE A SCHEDULE FOR MEASURING THE PROGRESS OF THE DESIGN AND DEVELOPMENT OF BIT. This should take the form of subdividing the hardware and software and requiring schedule for completion of BIT mechanization for each subdivision. For the software subdivisions, completion would mean a program has been written, debugged and verified. Completion for the hardware subdivision should include a paper analysis for proof of design, the form of which is currently undefined (see Research).

(8) THE CONTRACTOR AND PROGRAM OFFICE SHOULD DESIGNATE A SINGLE ENGINEERING MANAGER RESPONSIBLE FOR MEETING THE 100 PERCENT DIAGNOSTIC CAPABILITY. The responsibility should include "vertical testability," that is, ensuring compatibility between on-equipment fault detection and isolation levels and tolerances.

(9) WHERE SUBCONTRACTORS ARE INVOLVED, DIAGNOSTIC REQUIREMENTS FOR A GIVEN SUBSYSTEM SHOULD BE SELF-CONTAINED WITHIN THAT SUBSYSTEM.

(10) PLANNING SHOULD INCLUDE DEDICATED TIME IN A TEST FACILITY OR A DEDICATED TEST ARTICLE FOR BIT DEVELOPMENT. Due to the large number and combination of faults that could occur, currently it is necessary to go through an iterative test process to mature the BIT mechanization. The proposed approach is similar to the reliability test, analyze, and fix approach. In the case of complex weapon systems, there is probably a need for a dedicated system.

(11) THE CURRENT PRACTICE OF REQUIRING CONTRACTUAL DEMONSTRATION BEFORE DELIVERY FOR FIELD TESTS OF THE BIT CAPABILITY SHOULD BE CONTINUED. This would include verification that the automatic diagnostic objectives are being achieved. However, it would be necessary to ensure that the quantitative BIT test

criteria are compatible with the design criteria. The BIT design criteria are based on 100 percent of all maintenance incidents while the tests are against a limited set of incidents (generally termed BIT-addressable faults). Further, it is desirable to expand the current demonstration approach to include environmental effects and/or a representative set of field failures. However, the techniques are not currently available to accomplish this and research must be done to expand the testing approach.

(12) TESTING (PARTICULARLY OPERATIONAL TESTS) AND DATA COLLECTION SHOULD FOCUS ON THE 100 PERCENT DIAGNOSTIC CAPABILITY. Testing and data collection also should evaluate the specified parameters, namely, the identification of critical failures, the false alarm rate, the percentage of faults detected and isolated automatically or manually and their associated repair items, the unnecessary removal rate, and the adequacy of personnel (need for high skill personnel) considering all maintenance incidents.

(13) USE OF THE DIAGNOSTIC CAPABILITY THAT IS PLANNED FOR FIELD MAINTENANCE PERSONNEL SHOULD BE REQUIRED WHENEVER THERE IS A NEED FOR SYSTEM MAINTENANCE. This applies to maintenance performed by either the contractor or the Service (user), particularly during the development phase. A large data base is needed as early as possible to provide information for any BIT development. Thus, contractors should be required to use the diagnostic capability in acceptance and qualification tests and in the manufacturing and quality assurance processes to the maximum extent possible. In addition to contributing to the maturation of the diagnostic capability, it was suggested that greater contractor use of diagnostics in these processes could result in production cost savings.

(14) A PROGRAM TO MATURE THE DIAGNOSTIC CAPABILITY SHOULD BE PLANNED FOR THE EARLY FIELDIED PRODUCTION SYSTEMS. A two year maturation program should be planned for complex weapon systems with extensive BIT. This program should include provisions for on-site collection of diagnostic performance data with engineering follow-up to provide corrective actions.

C. RESEARCH AREAS

Areas where additional investigation, analysis, or research is required to improve the specification and test process for diagnostic capability, as well as the design of diagnostic capability, are listed below.

(1) It is necessary to identify terms that can be used to describe personnel skill requirements in design specifications and which can be quantitatively evaluated in test.

(2) It is necessary to develop the statistical methods that should be used for predicting and confirming of diagnostic system performance, particularly for BIT.

(3) It is necessary to supplement the existing Maintainability Demonstration Standard MIL-STD-471 to include procedures and environments that will yield results more representative of the BIT and total diagnostic capability that will be observed in the field. Approaches should be investigated for selecting faults for the maintainability demonstration that are not predicated using standard fault predictions or failure modes and effects analysis (perhaps a sample from operational data on similar systems or evaluation by "independent verification" similar to software).

(4) The use of non-volatile memories and memory inspection as part of the diagnostic capabilities should be investigated to aid the maintenance technician in system troubleshooting, particularly in identifying intermittent and environmentally related failures, and to reduce shop test time and test equipment complexity at higher levels of maintenance.

(5) The type of information that needs to be displayed to operators in the use of BIT and other diagnostics aids should be determined; especially, how the operator should be trained to use these data to convey symptoms to maintenance personnel.

(6) The approaches that could be used to specify, predict and evaluate false alarms and unnecessary removals must be developed.

(7) Acquisition approaches must be developed to determine contractor compliance with diagnostic requirements. Compliance should not be limited to MIL-STD-471 demonstration tests for BIT.

(8) The need for an organization structure to pull together all of the various activities (management procedures, technical training, T&E, etc.) that are on-going in the diagnostic area must be investigated. OSD was suggested as the focal point to organize and pull together this structure.

(9) A methodology for trade-offs between personnel skill, automatic and manual capabilities and shop automatic test equipment requirements must be developed.

(10) A standard terminology for the "diagnostic" area should be developed.

(11) The implications of the use of different performance levels of BIT peacetime and wartime applications, and the corresponding manpower and other support requirements should be investigated.

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FOREWORD

The BIT Workshop on Requirements and Specifications was held at the Institute for Defense Analyses in Arlington, Va. on February 11, 12 and 13, 1981. The workshop was sponsored by OSD, MRA&L (Manpower, Reserve Affairs and Logistics) and hosted by IDA. Attendance was by invitation of OSD and was limited to 40 participants so as to promote a free exchange of ideas and experiences. The attendees were welcomed to the IDA facility by Dr. Harry Williams, Director, Program Analysis Division, IDA. Mr. Martin Meth, OSD, introduced the workshop. A total of ten presentations were given, followed by meetings of three separate Panels and subsequent presentation of Panel reports.

ACKNOWLEDGMENTS

I am indebted to the participants from the industry organizations and service agencies who contributed their time and efforts toward the success of the BIT Workshop. I want to acknowledge the Institute for Defense Analyses, which hosted the meetings: Dr. Harry Williams, Program Analysis Division Director, and Ms. Jean Orlikoff; and Miss Eileen M. Doherty for her efforts in the publication of these proceedings. A special debt of gratitude is due to Mr. Donald Mileson of Mileson Associates, Inc. and Col. Thomas Musson, U.S. Air Force, who cheerfully helped me with all aspects of this Workshop and who significantly contributed to making this Workshop a success.

Martin Meth

GLOSSARY

A	Hornet Aircraft in Attack Configuration
AC	Aircraft
A/D	Analog to Digital
ADC	Air Data Computer
AEGIS	Acronym for a Navy surface-to-air missile system
AIS	Avionics Intermediate Shop (I-level test equipment)
AFSC	Air Force Systems Command
AFTEC	Air Force Test and Evaluation Center
ASD	Aeronautical Systems Division (of AFSC)
ASQC	American Society for Quality Control
ATE	Automatic Test Equipment
AUG	Radar Augmentation Set
BCN	Beacon Set
BIS	Navy Bureau of Inspection and Survey
BIT	Built-In Test
BITE	Puilt-In-Test Equipment
BIT/FIT	Built-In-Test/Fault Isolation and Test
CADC	Central Air Data Computer
CAM	HUD Camera
CDC	Control Data Corporation
CPE	Contractor Furnished Equipment
CND	Could Not Duplicate (i.e., in shop testing installation)
COM 1/2	Radio #1/#2
CPS	Cycles Per Second
CPU	Central Processing Unit
CSC	Communication System Control Set
CSMC	Combat System Maintenance Control (AEGIS)

D	Detect
DAC	Digital to Analog Converter
DEGD	Degrade
D-Level	Depot Level
D/L	Data Link
DSPL	Display
ECM	Electronic Countermeasures
ECP	Engineering Change Proposal
EDM	Engineering Development Model
ENR	Expected Number of Removals
E/O	Electro/Optical
EPG	European Participating Governments
EPI	Engine Performance Indicator
ET	Electronics Technician
ETE	External Test Equipment
EU	Electronic Unit
F-18	Hornet 'Fighter' Configuration
FA	False Alarm
FC	Fire Control
FCC	Fire Control Computer
FCES	Flight Control Electronic Set
FCS	Flight Control System
FCSA(B)	FCS Channel A (Channel B)
FD/FI	Fault Detection/Fault Isolation
FH	Flight Hours
FLIR	Forward Looking Infrared Set
FLU	Flight Line Unit
FMEA	Failure Mode and Effects Analysis
FOM	Figure of Merit
FSD	Full Scale Development
FSE	Navy Fleet Support Evaluation
GD	General Dynamics
GFE	Government Furnished Equipment
GSE	Ground Support Equipment

HARM	High Speed Anti-Radiation Missile
HF	High Frequency
HOL	Higher Order Language
HUD	Head Up Display
HSD	Horizontal Situation Display
I	Isolate
IBS	Interference Blanker Set
ICS	Intercom Set
IECMS	Integrated Engine Condition Monitoring System
IEEE	Institute for Electrical & Electronic Engineers
IFF	Identification--Friend or Foe
I-Level	Intermediate Level
ILS	Integrated Logistics Support (also Instrument Landing System)
INS(U)	Inertial Navigation System (Unit)
IOP	Input/Output Processor
IR&D	Internal R&D
JLC	Joint Logistics Commanders
K	Kilo (1000)
LBTS	Land Based Test Site (AEGIS)
LRU	Line Replaceable Unit
LST/SCAM	Laser SPA Tracker/Strike Camera Pod
MAD	Magnetic Azimuth Detector
MATE	Modular ATE
MC	Mission Computer
MCAIR	McDonnell Aircraft Company
MDC	McDonnell Douglas Corporation
M-Demo	Maintainability Demonstration
MFL	Maintenance Fault List
MI	Memory Inspect
MMD	Cockpit Master Monitor Display
MMH	Maintenance Manhours
MMP	Maintenance Monitor Panel (\bar{M} Panel)
MOT&E	Multinational OT&E

MRA&L	Manpower, Reserve Affairs and Logistics (OSD)
MTBF	Mean Time Between Failure (hours)
MTBR	Mean Time Between Removal (hours)
MTTR	Mean Time to Repair (hours)
MUX	Multiplex
MUX BUS	Avionic Digital Multiplex Bus
NABIT	Built-in-Test for Nonavionic Subsystems
NAC	Naval Avionics Center
NAVAIR	Naval Air Systems Command
NAVMAT	Naval Material Command
NAVSEA	Naval Sea Systems Command
NEC	Naval Engineering Center
NOSC	Naval Ocean Systems Center
NPE	Navy Preliminary Evaluation
NSWC	Naval Surface Weapons Center
OFP	Operational Flight Program
O-Level	Organizational Level
ORTS	Operational Readiness Test System (used with AEGIS)
OSD	Office of the Secretary of Defense
OT&E	Operational Test and Evaluation
Pto	BIT Performance Fault Threshold
RADC	Rome Air Development Center
RALT	Radar Altimeter Set
R&R	Remove and Replace
RCVR	Receiver
RDDI/LDDI	Right/Left Cockpit Digital Display Indicator
RETOK	(also RTOK) Retest Okay (i.e., without removal from operational installation)
Restrt	Restart BIT Test
RIU	Remote Interface Unit
RMRB	Reliability Maintainability Review Board
SDRS	Signal Data Recorder Set
SE	Support Equipment
SEM	Standard Electronic Modules

S-Level	Shop Level
Sixty-1	(Also 60-1) an Air Force maintenance reporting system
SMS	Stores Management Set
SPO	System Program Office
SRA	Special Replacement Assembly
SRU	Shop Replaceable Unit
ST/BIT	Self Test/Built-In Test
STFF	Self Test Fault Flag
TACAN	Tactical Air Navigation
TCN	TACAN Set
T.O.	Technical Order
TRA	Test Requirements and Analysis
Δt_s	Maintenance Time Saved
UFC	Cockpit Up-Front Control Panel
USOR	Utility to Save and Restore the Disk
V	Verify
VSWR	Voltage Standing Wave Ratio
WRA	Weapons Removable (Replaceable) Assembly

OPENING REMARKS

MARTIN METH, OSD, MRA&L

Mr. Meth is the Staff
Engineer for OSD,
MRA&L

The agenda for the BIT workshop is shown as Figure 1-1. Case studies and associated discussions are scheduled, followed by panel discussions and reports.

The scope of the workshop involves the areas of requirements for built-in-test and diagnostics, and the methods of testing to ensure that the requirements have been met. The specific objectives are to characterize current practices and results, to recommend improvements and methods for implementation, and to identify those areas where research is required.

Figure 1-2 is an extract from an Air Force report outlining the past history of many BIT equipments in which specific diagnostic requirements have not been met and also indicating the absence of specified values for certain parameters. This information indicates that there is much improvement to be made in the areas of specifying, verifying and testing BIT and diagnostics.

The process of system development is shown in Figure 1-3; the overall areas addressed in this workshop are circled in the Figure. The topics to be addressed by each of the three panels are shown in Figures 1-4, 1-5 and 1-6. Reports on these topics (and others as appropriate) will be presented to the full panel and other invited attendees at the conclusion of the workshop.

BUILT-IN-TEST (BIT) REQUIREMENTS AND
EVALUATIONS WORKSHOP



WEDNESDAY, FEB. 11, 1981

8:30 - 9:00	Check-In	
9:00 - 9:30	Introduction & Announcements	Martin Meth
9:30 - 10:00	Background - NAVMAT	George Neumann
10:00 - 10:15	Break	
10:15 - 12:00	Operational Testing - AFTEC	Maj. Vince Linden
12:00 - 1:00	Lunch	
1:00 - 2:15	F16 - General Dynamics	Gordon England
2:15 - 3:30	F16 FCS - Westinghouse	Roy Pyle/Jim Victor
3:30 - 3:45	Break	
3:45 - 5:15	F18 - McDonnell-Douglas	Bob Drummond/ Ed Meyer
5:15 - 6:00	AYK-14 - CDC	Wei Long Chen
6:30	Dinner, Ft. Myer	

THURSDAY, FEB. 12, 1981

8:00 - 8:30	Check-In	Martin Meth
8:30 - 9:00	ALQ-126 - Maint. Tech.	Ken Wilson
9:00 - 9:30	SPS-67 - NOSC/NAC	Mel Nunn/John Rogers
9:30 - 10:15	AEGIS/ORTS - RCA	Howard Boardman
10:15 - 10:30	Break	
10:30 - 12:00	BIT Studies - RADC	Tony Coppola/ Capt. Dan Gleason
12:00 - 1:00	Lunch	
1:00 - 1:30	Instructions to Panels	Martin Meth
1:30 - 5:00	Panel Discussions	Panels
5:00 - 6:00	General Panel Recap	Panel Chairman

FRIDAY, FEB. 13, 1981

8:30 - 9:00	Check-In	Martin Meth
9:00 - 10:45	Panel Reports	Panel Chairmen
10:45 - 11:00	Summary of Results	Martin Meth

Figure 1-1

BIT/SIT IMPROVEMENT PROJECT
PHASE 1 - RESULTS

NOMENCLATURE	TYPE SUBSYSTEM	% FAULT DETECTION		% FAULT ISOLATION (LRU)		% FALSE ALARMS	
		SPEC	STUDY	SPEC	STUDY	SPEC	STUDY
AV/ARN-118	TACAN	85 (A)	48	N/A	--	N.S.	0
<input checked="" type="checkbox"/> AV/APX-101	IFF TRANSPONDER	90	100 (B)	90	78	N.S.	33
AV/APN-185	DOPPLER	95	71 (C)	95	N/A	N.S.	14
AV/APN-190	DOPPLER	95	61 (C)	N/A	--	N.S.	10
<input checked="" type="checkbox"/> AV/AYK-6	COMPUTER	(D)	91	83	77	N.S.	38
* AGM-69A	SRAM AVIONICS	95	97	N/A	--	2	.1
AV/APG-63	RADAR	95	55	N.S.	30	N.S.	29
AV/ASN-109	INERTIAL NAV	95	56 (E)	95	UNK	N.S.	44 (E)
MADAR (C-5A)	INTEGRATED TEST	N.S. (F)	11	N.S. (F)	UNK	N.S. (F)	89
* CITS (B-1)	INTEGRATED TEST	95	96	75	85 (G)	3 (H)	4
AV/APQ-114	RADAR	UNK	20	N/A	--	UNK	12
AV/ARC-164	RADIO	N/A	--	N/A	--	N/A	--
(A) COLLINS DESIGN GOAL		(E) MAY NOT BE TOTALLY BIT RESULT					
(B) NO INDICATION OF NON-BIT DET.		(F) SPEC REQUIRED 80% AVAILABILITY					
(C) BIT DETECTED AND/OR CONFIRMED		(G) 97% TO 3 LRU'S					
(D) INCLUDED W/ISOLATION REQUIREMENT		(H) DEVELOPMENT SPEC ONLY					
* MET SPECS	<input checked="" type="checkbox"/> MARGINAL	N.S. = NOT SPECIFIED					

Figure 1-2

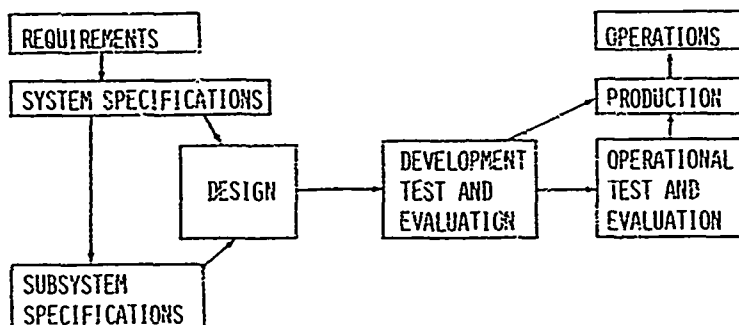


Figure 1-3

Figure 1-4

GROUP #1. REQUIREMENTS AND EFFECTIVENESS

THE RELATIONSHIPS BETWEEN BIT PERFORMANCE AND OPERATIONAL NEEDS FOR LOGISTICS AND MANPOWER REQUIREMENTS ARE NOT WELL UNDERSTOOD.

INADEQUATE RESOURCES AND UNREALISTIC SCHEDULES ARE BEING PROPOSED FOR DEVELOPMENT OF BIT.

GROUP #2. SUBSYSTEM SPECIFICATION AND TESTING

THE RESULTS OF CONTRACTOR BIT DEMONSTRATIONS (USING FAULT INSERTIONS) DOES NOT MATCH BIT PERFORMANCE IN THE FIELD

Figure 1-5

ANALYSIS OF BIT DESIGN EFFORTS ARE NOT PROVIDING DATA TO DETERMINE IF BIT SPECIFICATIONS CAN BE MET.

FUNDING AND SCHEDULE ALLOCATED FOR BIT DEVELOPMENT ARE GENERALLY NOT ADEQUATE.

GROUP #3. SYSTEM REQUIREMENTS AND TESTING

PERFORMANCE OF BIT IN THE FIELD IS GENERALLY MUCH LOWER THAN OBSERVED IN TESTING PRIOR TO PRODUCTION.

CURRENT APPROACHES TO BIT SYSTEM DESIGN DO NOT TAKE INTO ACCOUNT MANY REAL WORLD PROBLEMS AS EVIDENCED BY HIGH LEVELS OF FALSE ALARMS, UNDETECTED FAILURE, RETEST OK'S AND AMBIGUITIES.

BIT PERFORMANCE IN THE FIELD HAS NOT BEEN COMPATIBLE WITH PLANNED PERSONNEL SKILLS, TEST EQUIPMENT, AND OTHER LOGISTICS.

FUNDING AND SCHEDULE ALLOCATED FOR BIT DEVELOPMENT ARE GENERALLY NOT ADEQUATE

Figure 1-6

BIT PROGRAMS

George Neumann
NAVMAT-04T

Mr. Neumann is the technical director, test and monitoring systems program office of NAVMAT.

HIGHLIGHTS OF THE PRESENTATION

The primary objective of the various BIT programs is to develop improved methods of specifying and evaluating BIT. Recent relevant industry and service efforts addressing this objective are shown in Figure 2-1. The significant points are--

- These programs have brought the BIT, testability, and logistics problems to the attention of high level military and civilian personnel in the Department of Defense.
- BIT is viewed as a subset of testability.

The Navy BIT Workshop was held in December 1980 and included as participants: PMA 265 (F/A-18); OPTEVOR; NSIA Ad Hoc Automatic Testing Group; and the Navy Testing Technology Team. A report of the results of this workshop is available from NAVMAT-04T. The primary Navy BIT Workshop findings are shown in Figure 2-2. Significant points are--

- The BIT implementation problem is a management problem since technology is available.
- BIT requirements should reflect operational requirements.
- It is not realistic to prescribe across-the-board rates for fault detection, fault isolation, and false alarms.
- Advantage should be taken of knowledge-based systems.

Figure 2-3 presents a comparison of management-oriented recommendations which are the result of the Navy Ad Hoc Project, the Industry/Joint Services Automatic Test Project and the Navy BIT Workshop (December 1980), and lists those areas where such recommendations are being implemented by on-going efforts. An examination of Figure 2-3 indicates the absence of current efforts in certain areas that have been recommended for action. Significant points are--

- The Joint Service BIT Design Guide is to be reissued.
- Design for Testability Course is a two to three day course presented by NSWC for designers of weapons systems.

Figure 2-4 presents a comparison, among the three BIT Programs, of recommended tools for implementing testability requirements together with a statement of current efforts in these areas. Current efforts are underway in all areas addressed. Finally, Figure 2-5 presents a comparison of technical recommendations. There are no current efforts underway in the areas of vertical testability, "smart" BIT, and BIT calibration. It is significant to note that the time required in operational use to "mature" the BIT (i.e., to tailor the BIT to an operational environment and to utilize it most effectively) may be two to three years.

A summary of the requirements of an effective BIT program is as follows:

A BIT program is required which tracks the weapon system acquisition cycle and includes--

- Management and user involvement including realistic specification, closed-loop tracking and reporting;
- Continued development of standards, specifications, guides and tools;
- Technology development.

DISCUSSION POINTS

- Experience with fielded systems has indicated a BIT false alarm rate between 20 to 30 percent in RADC studies.
- Other RADC studies involving nine different Air Force systems at numerous bases have shown unnecessary removal rates on the order of 40 percent with some systems as high as 89 percent.
- Multiple "box-swapping" maintenance practices are used in the field because of shortcomings in BIT, according to RADC studies of Air Force systems.
- False alarms are sometimes defined as "something the operator learns to ignore."
- False alarms may indicate a true fault that does not require immediate correction.
- False alarms may indicate degradation trends, particularly if their interarrival periods are decreasing.
- False alarms may indicate intermittent failures as shown by CND (could not duplicate) and RETOK (retest okay) rates.
- Airlines find that far less than 50 percent of boxes removed contain verified failures, especially autopilots (the worst) which run 85 to 90 percent non-verified.
- The increased rate of false alarms in the autopilot systems probably reflects the criticality of this system and the fact that it is more heavily monitored by BIT than other, less critical, systems.
- Another problem with autopilots is CND's on the ground, partly because of the inability to reproduce the flight environment on the ground (e.g. "porpoising" in the pitch axis). Many unnecessary replacements of the pitch computer result.
- Autopilot "squawks" are often identified by pilots as a defect in a major unit that may not be at fault.
- BIT systems up to now have been widely ignored by airline maintenance people because of the lack of agreement between BIT fault indications and flight crew "squawks."
- Airlines are requiring BIT in new systems to incorporate fault diagnostic memories to address intermittents, with user options as to how many flight legs are recorded along the lines of "smart" BIT.

- The airlines are asking that in future complex systems BIT be implemented using a master LRU with an alpha-numeric readout identifying the failed unit and its future mode.
- The need for rapid turnaround time for the airlines results in many unnecessary removals and replacements of units. This, in turn, results in the requirement for increased spares. BIT presently has little effect on this because it is generally ignored.
- Airline pilots are often drivers of unit replacements (possibly unnecessarily) because they insist that the unit be replaced, particularly in radar systems.
- The new NAVAIR maintainability standard presently in progress contains certain numerical requirements. This approach must be reviewed carefully before publishing the standard.

Figure 2-1

RELEVANT INDUSTRY/SERVICE EFFORTS

- **INDUSTRY AD HOC ATE PROJECT FOR THE NAVY**
- **INDUSTRY/JOINT SERVICES AUTOMATIC TEST PROJECT**
- **AFTEC STUDY (AUTOMATIC DIAGNOSTIC SYSTEMS)**
- **NAVY BIT MINI-WORKSHOP**
- **JLC/NAVY CURRENT EFFORTS**

Figure 2-2

NAVY WORKSHOP FINDINGS

- **TECHNOLOGY EXISTS: BIT DEVELOPMENT IS A MANAGEMENT PROBLEM**
- **BIT REQUIREMENTS SHOULD REFLECT OPERATIONAL REQUIREMENTS: ACROSS THE BOARD OR STANDARD FD/FI/FAR PERCENTAGES NOT A REALISTIC APPROACH**
- **BIT ALLOCATION IS INFLUENCED BY OTHER FACTORS (E.G.: RELIABILITY, MAINTAINABILITY, MANNING)**
- **BIT DEVELOPMENT IS AN ITERATIVE PROCESS**
- **ADAPTIVE DESIGN IS LAGGING: "SMART" BIT NEEDS TO BE DEVELOPED**

Figure 2-3

COMPARISON OF RECOMMENDATIONS (MANAGEMENT)

NAVY AD HOC PROJECT	I/JSATP	WORKSHOP	CURRENT EFFORTS
<ul style="list-style-type: none"> • IMPLEMENT MORE EFFECTIVE POLICIES 	<ul style="list-style-type: none"> • IMPLEMENT MORE EFFECTIVE POLICIES • CONTRACTOR INCENTIVES 	<ul style="list-style-type: none"> • ESTABLISH REALISTIC BIT REQUIREMENTS • CONTRACTOR INCENTIVES • MANAGEMENT EDUCATION • SYSTEM-LEVEL FOCAL POINT • CLOSED-LOOP DATA COLLECTION SYSTEM • EARLY USER INVOLVEMENT IN BIT TEST & EVALUATION (OPNAVINST 3960.10) 	<ul style="list-style-type: none"> • NAVMATINST 3960.9A • <u>DESIGN FOR TEST-ABILITY COURSE</u> WHICH INCLUDES DISCUSSION OF BIT
<ul style="list-style-type: none"> • T AUDIT & REVIEW 	<ul style="list-style-type: none"> • T AUDIT & REVIEW 	<ul style="list-style-type: none"> • BIT AND R DESIGN REVIEWS • CONTINUOUS EVALUATION OF BIT PERFORMANCE 	<ul style="list-style-type: none"> • NAVMATINST 3960.4B

Figure 2-4

COMPARISON OF RECOMMENDATIONS (TOOLS)

NAVY AD HOC PROJECT	I/JSATP	WORKSHOP	CURRENT EFFORTS
<ul style="list-style-type: none"> • T SPECIFICATIONS & MEASURES 	<ul style="list-style-type: none"> • T SPECIFICATION REQUIREMENTS • TFOMS • DEFINITION OF TERMS 	<ul style="list-style-type: none"> • T MIL-STD • TFOMS/BIT FOMS • DEFINITION OF TERMS 	<ul style="list-style-type: none"> • T MIL-STD BEING DEVELOPED, ADDRESSING BIT AS IT RELATES TO T • ESTABLISHMENT OF T FIGURES OF MERIT (TFOMS) • MIL-STD-1309C
<ul style="list-style-type: none"> • REVIEW BIT DESIGN GUIDE 		10	<ul style="list-style-type: none"> • JOINT SERVICE BIT DESIGN GUIDE HAS BEEN DEVELOPED

Figure 2-5

COMPARISON OF RECOMMENDATIONS (TECHNICAL)

NAVY AD HOC PROJECT	I/JSATP	WORKSHOP	CURRENT EFFORTS
<ul style="list-style-type: none"> • CONTINUING BIT R&D <ul style="list-style-type: none"> - LSI - WRA - SUBSYSTEMS 	<ul style="list-style-type: none"> • INVESTIGATE DISTRIBUTED BIT • MILITARY T <ul style="list-style-type: none"> - VERTICAL COMMON-ALITY - REDUCE FALSE ALARMS 	<ul style="list-style-type: none"> • INTEGRATE BIT WITH REDUNDANT DESIGN TECHNIQUES • VERTICAL COMMONALITY • DEVELOP "SMART" BIT • BIT CALIBRATION PROGRAM 	<ul style="list-style-type: none"> • ADDRESS COMPONENT BIT/T ISSUES IN OSD VHSIC PROGRAM • FAULT TOLERANT DESIGN TECHNIQUES

TRENDS AND FUTURE APPROACHES IN AUTOMATED DIAGNOSTICS

Major Vince Linden
AFTEC

Major Vince Linden is the
OT&E Logistics Assessment
Policy Manager for AFTEC.

HIGHLIGHTS OF THE PRESENTATION

The purpose of the presentation is to discuss trends towards highly automated diagnostics for maintenance personnel in the field, recent OT&E results, and impacts on planned maintenance and training concepts; and to discuss future approaches towards the acquisition of diagnostic systems. The approach used to achieve this purpose is through presentation of BIT background information, discussion of diagnostic theory, and a display of E-3A, F-16 and EF-111A BIT test results.

BIT trends in the 1970s in terms of personnel and systems are shown in Figure 3-1. Training and maintenance concepts and the expected results based on the trends of the 1970s are shown in Figures 3-2 and 3-3. First term productivity means "first enlistment.") However, because of inadequate performance of BIT, the actual impacts are as shown in Figures 3-4 and 3-5. The increases shown are those above the planned requirements, due primarily to the fact that the systems (including BIT) are not mature. The problems with OT&E as indicated in Figure 3-5 derive from the fact that the systems have not been tested by the contractor as the system's diagnostics would be used in an operational environment. In many cases, Tech Orders (Manuals) are not available for use in maintenance by the contractor. Use of immature diagnostics slow down contractor's testing and cost him time and money. In addition, the government has not yet been able to properly articulate diagnostics requirements to contractors.

Improved methods for use of diagnostics have been applied to the E-3A and subsequently enhanced for application to the F-16 and EF-11A as indicated in Figure 3-6. The two types of systems used in the F-16 to which BIT is applied are shown in this Figure. The flight control system is primarily an analog system whereas the "MUX BUS" is a digital system.

Fault detection and isolation requirements are shown in Figure 3-7. These can be met by incorporating 100 percent fault detection in units 1 through 5 and 100 percent fault isolation in units 1 through 4. Breakdowns between automatic and manual fault detection and isolation are as shown. The numbers shown must be precisely defined since they can mean different things to the contractor and the government. No values have been shown for CNDs, RETOKs, and false alarms. The term "CND" is used to identify the situation where 0-level maintenance is not able to reproduce the "squawk" reported by the flight crew on BIT. The term "RETOK" is used to identify the situation where 0-level maintenance has verified the reported fault but I-level maintenance has tested the unit and found no fault. In this case, the problem was apparently solved by the replacement of the "squawked" unit. Repair times (MTTR) need to be specified for both automatic and manual modes as well as the percentage of actions in each mode. Special category data (or events) are defined as non-addressable events and have not been included for this analysis; specifically these category data include human error, other maintenance, cannibalizations, deferred maintenance, interrelated failures, and BIT/FIT-pertinent data discovered during trouble shooting.

It is important to know the elements of MTTR in order to focus on the problem of high MTTR and unsatisfactory turnaround time. In some cases, systems in the field have horrible maintainability problems but the maintenance people are keeping the system up at an excessively high cost in resources. For

example, one LRU in the E-3A requires a hoist and pulley system to remove it from the aircraft, resulting in a very high remove/replace time.

As BIT/FIT becomes more successful, the fault detection isolation portion of MTTR becomes a smaller and smaller percentage of MTTR. However, when BIT/FIT is not successful, the "beyond BIT" maintenance becomes increasingly more difficult and requires higher skill level personnel. Properly trained people and adequate T.O.s are often not available to provide such maintenance when it is needed. In addition, different BIT/FIT systems will differ in diagnostic characteristics according to definitional differences, mechanization and system design. In some cases, maintenance policies will also mask the true diagnostic capability.

The data base used to obtain E-3A test results is shown in Figure 3-8; E-3A radar events are shown in 3-9; and radar maintenance events are shown in Figures 3-10 and 3-11. Only the surveillance radar of the E-3A is included in this analysis. Certain false alarms are presently being tracked for possible trend analysis to detect degradation in unit performance. Fault isolation in the E-3A is off-line, requiring transfer of the diagnostic programs for execution. Addressable events are shown in Figure 3-12, indicating the effect of CNDs on detection and non-detection percentages as viewed by the government and the contractor; and the effect of RETOKs on isolation percentage as viewed by the government and the contractor. As can be seen, CND and RETOK requirements were not imposed on the contractor for the E-3A. The actual auto-isolation percentage is shown to be between 34 and 49 percent. Some of the RETOKs were actually bad but no problem could be found at the repair facility. The RETOK rate was essentially the same whether fault isolation was automatic or manual (about 30 percent).

The AFTEC tests were started two years after the E-3A had been in the field. The test was conducted by the Air Force with the assistance of Boeing and Westinghouse Engineering support personnel. The data are considered highly accurate since they were checked by Air Force Test Team personnel prior to entry into the data base.

The original E-3A spec requirements of 98 percent automatic fault detection, 95 percent automatic fault isolation were reduced to 90/79 percent respectively.

The impact to the E-3A as a result of inadequate diagnostics are shown in Figure 3-13. In-flight repair was not evaluated during the test period since only 21 attempts at in-flight repair were documented and, of these, only two were successful. Spares are carried on-board the E-3A to effect in-flight repair. However, the radar must be shut down for repair actions and this was usually not done due to mission impacts. Maintainability deficiencies have been largely overcome due to extraordinary supply measures, employed by the 552 AWACW and the E-3A system manager. Additional TOs (manuals) have been required both for the system and its support equipment.

Extensive additional training requirements have been experienced and documented by the Wing. As a result, the Air Force must track individual personnel qualifications for assignment to various E-3A units.

The data base used to obtain the F-16 test results are shown in Figure 3-14. The characteristics of the two different types of systems (flight control and MUX-BUS) are shown in Figure 3-15. Several comments are in order: Flight control data (fly-by-wire, totally electronic) are not polluted by data from interactions among systems. The MUX-BUS incorporates many systems. Fault detections in the flight control

are presented to the pilot who must record the fault indications, as opposed to the MUX-BUS which records the faults in memory for later readout. As a result, some of the faults (particularly intermittents) are missed in the analog flight control system.

Figure 3-16 shows the box score reflecting the ST/BIT (self-test, built-in-test) performance of the F-16 flight control system (a quad-redundant system), as seen by the contractor and by the user. Operational experience indicates that both reliability and maintainability are improved the more aircraft is flown.

Figure 3-17 shows a similar box score for the F-16 MUX BUS. The fault reporting on the MUX BUS does not include failures of input devices to the units on the MUX BUS (e.g., angle of attack unit as an input to the CADC). Correction of this deficiency requires imposing testability requirements on the units (e.g., CADC) and impacts requirements for GFE.

The impacts of F-16 ST/BIT shortfalls or inadequate diagnostics point to several problems: There is a need for additional trouble-shooting guides; the training courses need restructuring; there appear to be Avionics Intermediate Test Station (AIS) compatibility problems; and many support decisions are still uncertain.

Figure 3-18 shows the extent of the EF-111A test effort, a modest effort compared to the E-3A and the F-16. Figures 3-19 and 3-20 indicate the results of the testing. The impacts of the EF-111A BIT/BITE are too early to determine. This system will be tested in depth during the October-December 81 timeframe.

Conclusions and recommendations are shown in Figures 3-21 through 3-26. General conclusions are that user-command personnel must become more involved in defining deployment/

employment concepts and operational and maintenance constraints, and in defining his requirements. One hundred percent diagnostic capability is required using both automatic and manual diagnostics.

Figure 3-1

BACKGROUND

TRENDS IN THE 1970s

- PERSONNEL INSTABILITY - HIGH TURNOVER
- TRAINING COST INCREASES
- FIRST TERM PRODUCTIVITY INCREASE NEEDED
- OPERATIONAL READINESS IMPROVEMENTS NEEDED
- LIFE CYCLE COST REDUCTION EMPHASIZED
- TECHNOLOGICAL ADVANCES
 - MICRO PROCESSORS
 - "SMART" DIAGNOSTIC SYSTEMS
- HEAVY INVESTMENT IN SOPHISTICATED BIT
- TRAINING AND MAINTENANCE CONCEPTS DEVELOPED AROUND BIT

Figure 3-2

BACKGROUND

BIT TRAINING CONCEPT

- ASSUMPTIONS
 - BIT CAN ELIMINATE NEED TO TEACH SYSTEM THEORY
 - LONG TECHNICAL SCHOOLS DRIVE TRAINING COSTS
 - OPERATIONAL COMMANDS NEED GREATER FIRST TERM PRODUCTIVITY
- ACTIONS
 - PROVIDING ONLY TASK ORIENTED/BIT DIRECTED TRAINING
 - DOING MAXIMUM TRAINING AT FIRST OPERATIONAL BASE
- EXPECTED RESULTS
 - REDUCED FIRST TERM FORMAL SCHOOLING
 - INCREASED FIRST TERM PRODUCTIVITY

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Figure 3-3

BACKGROUND

BIT MAINTENANCE CONCEPT

- ASSUMPTIONS
 - BIT CAN REDUCE TROUBLE SHOOTING TIME
 - BIT CAN REDUCE SUPPORT EQUIPMENT REQUIREMENTS
- ACTIONS
 - TECHNICAL DATA WRITTEN AROUND BIT OPERATION
 - SUPPORT EQUIPMENT NOT PROCURED
- EXPECTED RESULTS
 - REDUCED MANNING
 - INCREASED OPERATIONAL READINESS
 - REDUCED LIFE CYCLE COST

Figure 3-4

BACKGROUND

PROBLEM WITH THE CONCEPTS

- BIT SYSTEMS FAILED TO PERFORM ADEQUATELY
- IMPACTS
 - EXTENSIVE ADDITIONS TO TECH DATA
 - ADDITIONAL TRAINING
 - SUPPLEMENTAL SUPPORT EQUIPMENT
 - MORE TECHNICIANS
 - CONTINUING CONTRACTOR SUPPORT
 - + \$

6-9-81.5

Figure 3-5

BACKGROUND**OT&E EXPERIENCE**

- INCOMPLETE, IMMATURE DIAGNOSTICS
- RARELY USED BY CONTRACTOR
- DIAGNOSTIC SPECIFICATIONS NOT MEANINGFUL
- IMPROVED EVALUATION METHODOLOGY NEEDED

Figure 3-6

DIAGNOSTIC THEORY**FD/FI TERMINOLOGY**

PROGRAM		FAULT DETECT (FD)	FAULT ISOLATE (FI)
E-3A		BIT	FIT
F-16	FLIGHT CONTROL	ST/BIT	BIT
	MUX BUS	BIT	BIT
EF-111A		BIT/BITE	BIT/BITE

6-9-81-6

Figure 3-7

DIAGNOSTIC THEORY

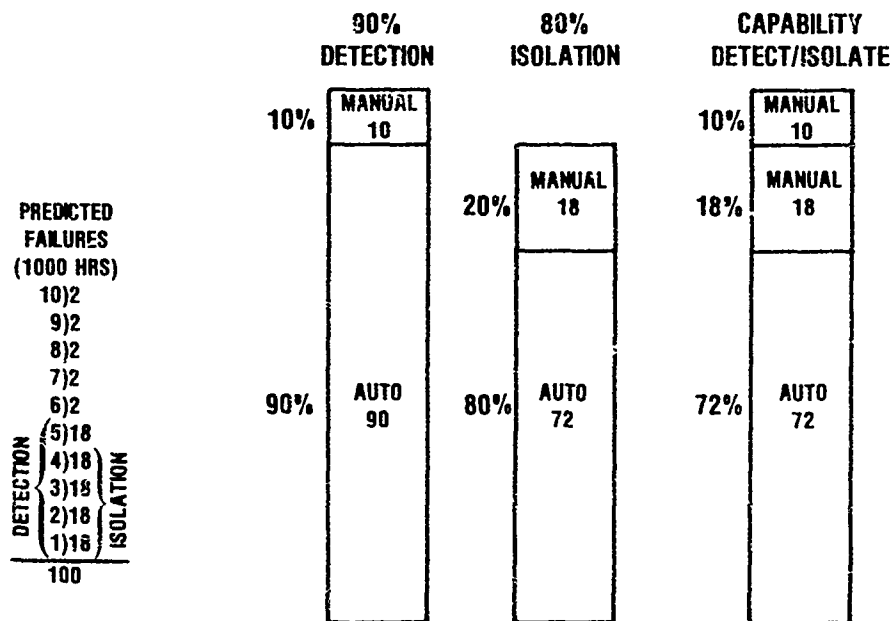
THEORY FOR DESIGNING A 90/80%
FD/FI CAPABILITY

Figure 3-8

TEST RESULTS

E-3A TEST RESULTS

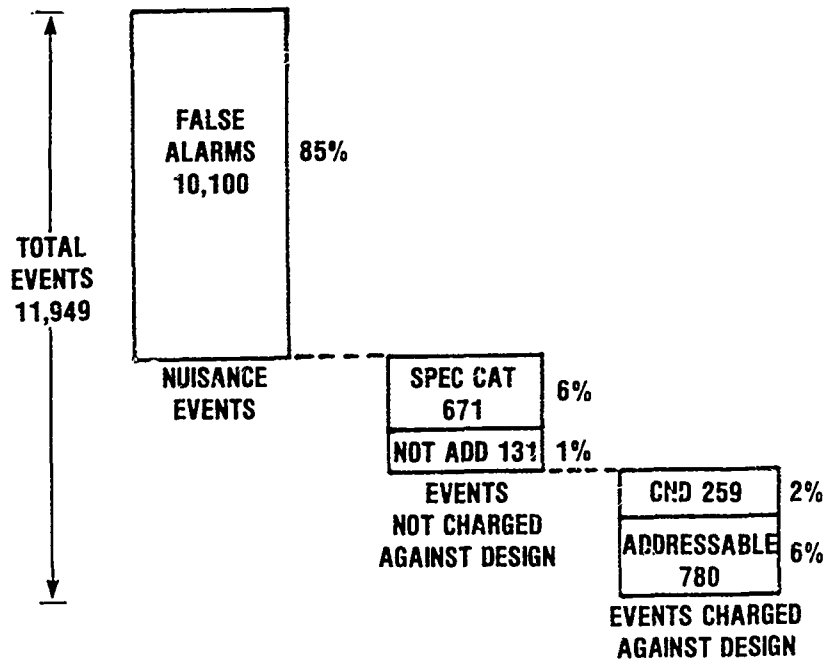
- DATA BASE
 - 19 AIRCRAFT
 - 18 MONTHS (JUL 78 - DEC 79)
 - 791 SORTIES
 - 6,205 FLYING HOURS
- DEDICATED BIT/FIT TEST TEAM
- TINKER AFB OK

6-9-81-7

Figure 3-9

TEST RESULTS

E-3A RADAR EVENTS



6-9-81-8

Figure 3-10

E-3A RADAR MAINTENANCE EVENTS

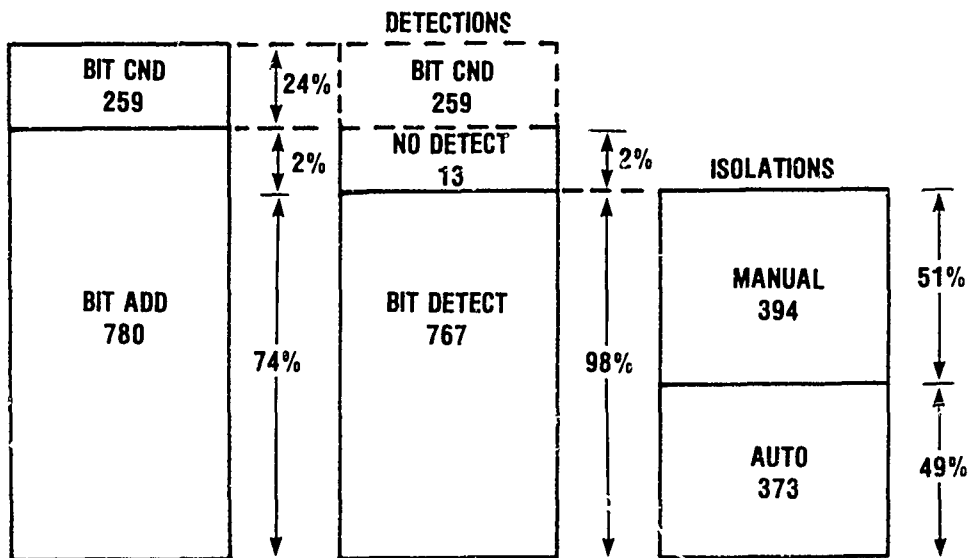


Figure 3-11

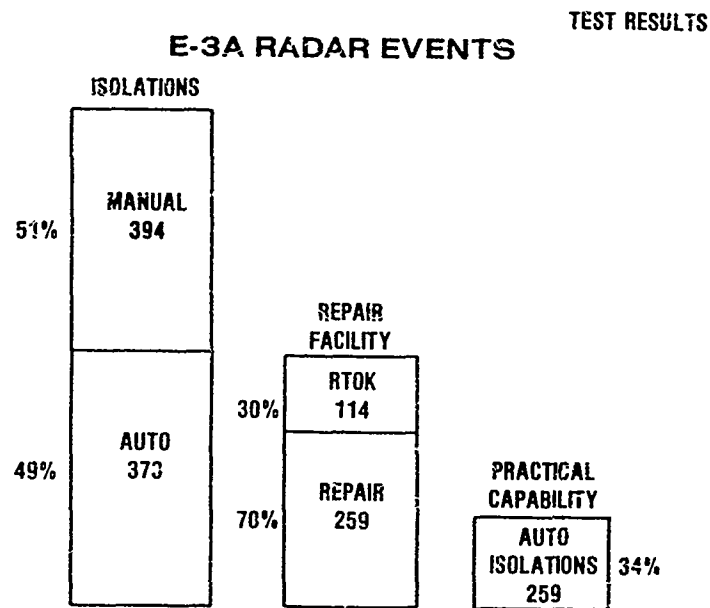


Figure 3-12

TEST RESULTS

E-3A RADAR BIT/FIT PERFORMANCE

MEASURE OF EFFECTIVENESS	RESULTS		RATING	
	AS CONTRACTOR SEES IT	AS USER SEES IT	AS CONTRACTOR SEES IT	AS USER SEES IT
FAULT DETECTION (%)	98	74	EXCELLENT	DEFICIENT
CANNOT DUPLICATE (%)	—	25	—	DEFICIENT
FAULT ISOLATION (%)	49	34	DEFICIENT	DEFICIENT
RETEST OKAY (%)	—	30	—	DEFICIENT

6-9-81-9

Figure 3-13

TEST RESULTS

E-3A BIT/FIT SHORTFALL IMPACTS

- INFLIGHT REPAIR NOT USED
- 18 ADDITIONAL RADAR TOs DEVELOPED
- 9 ADDITIONAL SUPPORT EQUIPMENT TOs DEVELOPED
- ADDITIONAL SUPPORT EQUIPMENT NECESSARY
- 6 ADDITIONAL TRAINING MONTHS (6 COURSES)
- 25 ADDITIONAL MONTHS IN OJT REQUIRED

Figure 3-14

TEST RESULTS

F-16 TEST RESULTS

- DATA BASE
 - 13 AIRCRAFT
 - 18 MONTHS (JAN 79 - JUN 80)
 - 2899 SORTIES
 - 3825 FLYING HOURS
- PART OF F-16 OPERATIONAL SUITABILITY FOT&E
- HILL AFB UT

8-9-81-10

Figure 3-15

TEST RESULTS

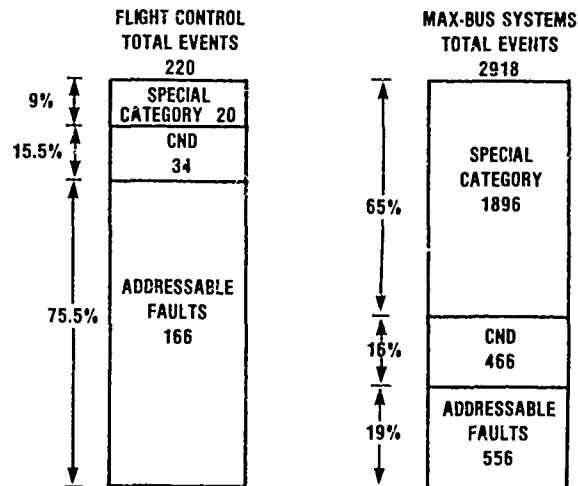
F-16 ST/BIT EVENTS

Figure 3-16

TEST RESULTS

F-16 FLIGHT CONTROL ST/BIT PERFORMANCE

MEASURE OF EFFECTIVENESS	RESULTS		RATING	
	AS CONTRACTOR SEES IT	AS USER SEES IT	AS CONTRACTOR SEES IT	AS USER SEES IT
FAULT DETECTION (%)	100	83	EXCELLENT	DEFICIENT
CANNOT DUPLICATE (%)	—	17	—	DEFICIENT
FAULT ISOLATION (%)	92	73.6	EXCELLENT	DEFICIENT
RETEST OKAY (%)	—	20	—	DEFICIENT

6-9-81-11

Figure 3-17

TEST RESULTS

F-16 MULTIPLEX BUS RESULTS

MEASURE OF EFFECTIVENESS	RESULTS		RATING	
	AS CONTRACTOR SEES IT	AS USER SEES IT	AS CONTRACTOR SEES IT	AS USER SEES IT
FAULT DETECTION (%)	90	49	SATISFACTORY	DEFICIENT
CANNOT DUPLICATE (%)	—	45.6	—	DEFICIENT
FAULT ISOLATION (%)	93	69	SATISFACTORY	DEFICIENT
RETEST OKAY (%)	—	25.8	—	DEFICIENT

Figure 3-18

TEST RESULTS

EF-111A TEST RESULTS

• DATA BASE

- 1 AIRCRAFT
- 5 MONTHS (APR-OCT 79)
- 86 SORTIES
- 261 FLYING HOURS

• PART OF EF-111A FOT&E

• MT HOME AFB ID

Figure 3-19

EF-111A EVENTS

TEST RESULTS

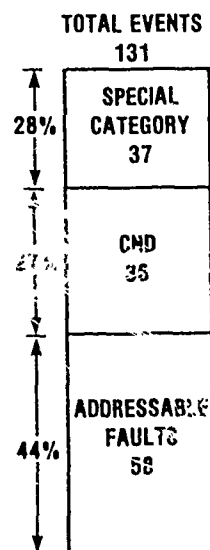


Figure 3-20

EF-111A BIT/BITE PERFORMANCE

TEST RESULTS

MEASURE OF EFFECTIVENESS	RESULTS		RATING	
	AS CONTRACTOR SEES IT	AS USER SEES IT	AS CONTRACTOR SEES IT	AS USER SEES IT
FAULT DETECTION (%)	100	62	—	—
CANNOT DUPLICATE (%)	—	38	—	—
FAULT ISOLATION (%)	88	71	—	—
RETEST OKCY (%)	—	19.2	—	—

6-9-81-13

Figure 3-21

CONCLUSIONS AND RECOMMENDATIONS

WHAT DO WE TELL USERS?

- DEVELOP DEPLOYMENT/EMPLOYMENT CONCEPTS
- DETERMINE THE OPERATIONAL AND MAINTENANCE CONSTRAINTS
 - DOWN TIME
 - SKILL LEVEL
 - MANPOWER
 - TRAINING
 - SUPPORT EQUIPMENT
- DEVELOP REQUIREMENTS BASED ON CONSTRAINTS
 - MAXIMUM REPAIR TIME ALLOWABLE
 - MEAN TIME TO REPAIR
- DO NOT SPECIFY FD/FI PERFORMANCE IN TERMS OF TRADITIONAL NUMERIC VALUES
- INSIST ON 100% DIAGNOSTIC CAPABILITY
 - MIXTURE OF AUTOMATIC AND MANUAL DIAGNOSTICS

Figure 3-22

CONCLUSIONS AND RECOMMENDATIONS

WHAT DO WE TELL DEVELOPERS?

- DEVELOP FD/FI SPECIFICATIONS BASED ON USER REQUIREMENTS AND CONSTRAINTS
- REQUIRE 100% DIAGNOSTIC CAPABILITY
 - MIX OF AUTOMATIC AND MANUAL DIAGNOSTIC CAPABILITY
 - COMPENSATION FOR SHORTFALLS IN AUTOMATIC CAPABILITY
- REQUIRE VERTICAL TESTABILITY
- UNDERSTAND LIMITS OF CURRENT TECHNOLOGY
- REQUIRE AN INTEGRATED DIAGNOSTIC PLAN
 - MILESTONES
 - SUPPORT OR DEVELOPMENT FACILITY
 - SPECIAL TEST INSTRUMENTATION
 - SYSTEM DEMONSTRATION UNDER OPERATIONAL CONDITIONS
 - MATURATION PROGRAM
 - CLOSED LOOP DATA SYSTEM

6-9-8.-14

Figure 3-23

CONCLUSIONS AND RECOMMENDATIONS

WHAT DO WE TELL CONTRACTORS?

- INSURE MANAGERS CONSIDER:
 - DIAGNOSTICS AS SYSTEMS ENGINEERING DISCIPLINE
 - THE INTERRELATIONSHIPS OF DIAGNOSTICS TO OTHER ILS ELEMENTS
 - THE NEED TO USE DIAGNOSTICS DURING DT&E/OT&E
- INSURE DESIGNERS CONSIDER:
 - THE NEED FOR PARALLEL DEVELOPMENT OF DIAGNOSTICS AND HARDWARE
 - STRATEGIES TO MINIMIZE THE OCCURRENCE OF FALSE ALARMS, CNDs AND RTOKs
 - FAILURE MODES EXPERIENCED IN THE OPERATIONAL ENVIRONMENT

Figure 3-24

CONCLUSIONS AND RECOMMENDATIONS

WHAT DO WE TELL AIR STAFF?

- RECOGNIZE THAT DIAGNOSTIC CAPABILITY, NOT DEGREE OF AUTOMATION, IS THE ISSUE
 - SYSTEM TRAINING STILL REQUIRED
 - AUTOMATION TECHNOLOGY STILL EVOLVING
- DESIGNATE A MANAGEMENT ORGANIZATION WITHIN THE AIR
 - CENTRAL REPOSITORY AND CORPORATE BODY OF KNOWLEDGE
 - REVIEW AND PROVIDE GUIDANCE ON DOCUMENTATION ADDRESSING DIAGNOSTICS
 - STANDARDIZE TERMINOLOGY

8-9-81-15

Figure 3-25

CONCLUSIONS AND RECOMMENDATIONS

WHAT DO WE TELL TESTERS?

- GET INVOLVED EARLY
 - UNDERSTAND SYSTEM DESIGN AND CAPABILITIES
 - PLAN FOR SPECIAL TEST INSTRUMENTATION
 - DEVELOP ANALYTICAL TOOLS
 - IDENTIFY CONTRACTUAL DATA REQUIREMENTS
- RECOGNIZE THAT TRADITIONAL MAINTAINABILITY DEMOS ARE INADEQUATE
- PLAN FOR SEQUENTIAL TESTING TO TRACK SYSTEM MATURATION
- EMPLOY A SINGLE THREAD, CLOSED LOOP DATA SYSTEM TO INSURE TRACEABILITY

Figure 3-26

SUMMARY

- 100% DIAGNOSTIC CAPABILITY REQUIRED
 - AUTOMATION SHORTFALLS RECOGNIZED TOO LATE
 - SIGNIFICANT MISSION IMPACT
 - PROBLEMS PERSIST FOR LONG PERIODS
 - WORKAROUNDS NOT ADEQUATE
 - ORIGINAL MAINTENANCE AND TRAINING CONCEPTS INVALIDATED
- MANAGEMENT ATTENTION AT THE HIGHEST LEVEL IS REQUIRED NOW
- DIAGNOSTIC "CORPORATE BODY" ESSENTIAL

1-81-18

ADDENDUM TO AFTEC BRIEFING

Major Robert Shafer
F-16 Suitability Team

Major Bob Shafer is the
Chief of the F-16 Suita-
bility ST/BIT Evaluation
Team at Hill AFB, Utah.

HIGHLIGHTS OF THE PRESENTATION

The difference between automatic and manual trouble shooting for the MUX BJS is not significant in terms of MTTR (2.71 hours vs. 2.05 hours) as shown in Figure 3-27. However, the difference between automatic and manual trouble shooting for the flight control system is highly significant in terms of MTTR (11.07 hours vs. 3.63 hours) as shown in Figure 3-28. A flight line tester is required for the flight control system to complete fault isolation to the failed component within the functional area identified by the in-flight BIT. Addressable faults in the flight control system included 166 events.

DISCUSSION POINTS

- Several airline studies have indicated the presence of chronic defective units such that 90 percent of the problems are caused by 10 percent of the units. This experience was confirmed by Air Force work with inertial navigation systems.
- Airlines have found that certain aircraft with cabling defects also contribute to high CND rates.
- The airlines are looking to BIT to provide shop qualification for checkout of avionics units (including regulatory problems).
- Carnegie Mellon has done some preliminary work on trend analysis concerning interarrival rates of false alarms indicating deterioration of system performance when interarrival times decrease, permitting prediction of times for removal of units, prior to any detection of such degradation by the pilot. Tracking by serial number is required to provide this information.

- Tightening of the parameter ranges for fault detection can increase false alarm rates excessively.
- False alarms degrade confidence in the BIT, sometimes resulting in the flight crew ignoring actual failures.
- Contractors in RADC studies have found that the quality of the data from 3M and 60-1 is inadequate to perform the analyses required. A special closed-loop monitoring system is required for new complex systems.
- Ambiguous fault isolation can result in the replacement of multiple boxes (some good, some bad) in order to restore the system. Some unit or SRA swapping reduces the number returned for I-level repair.
- Imposition of CND and RETOK requirements are dependent on maintenance philosophy and are difficult or impossible to impose on subcontractors.
- Selection of faults for maintainability tests must be randomly selected from a large number of comprehensively defined faults, including cable faults and others that are representative of the operational environment such as inputs from and outputs to other interfacing equipments.
- Support philosophy and training requirements are developed based on maintainability predictions; differences between predictions and reality can cause significant impacts in support and training.
- The airlines are accumulating data bases of characteristics of reliabilities demonstrated and fault isolation capabilities on different types of units (LRU's, circuit boards, etc.) in order to determine realistic characteristics to expect for these items in the future. In digital board testing, the isolation capability has been around 43 percent vs. 90 percent claimed.
- Some of the larger airlines do not buy diagnostic software from the vendors but build it themselves after delivery when the hardware is completed.
- The airlines use A&P personnel for flight line maintenance, reserving more highly qualified personnel for shop maintenance.
- The trend as shown in the E-3A is from the "smart machine, dumb man" to the "smart machine, smart man" concept to cover the areas where BIT fails to detect and isolate the problem.

- The airlines have had better BIT experience with digital units than they have with analog units, although they have little or no experience with multiplexing these units on a data bus.
- Backplanes and pin quality are important contributors to the intermittents (e.g., "RADC Backplanes" in the EF-111). The F-15 has high quality (and expensive) pins and wiring. These have been degraded in the F-16 by the Air Force as an economy measure and may cause future problems.

MUX-BUS SI/BIT FAULT DETECT/FAULT ISOLATE MTTR ANALYSIS

JAN 1979 - JUN 1980

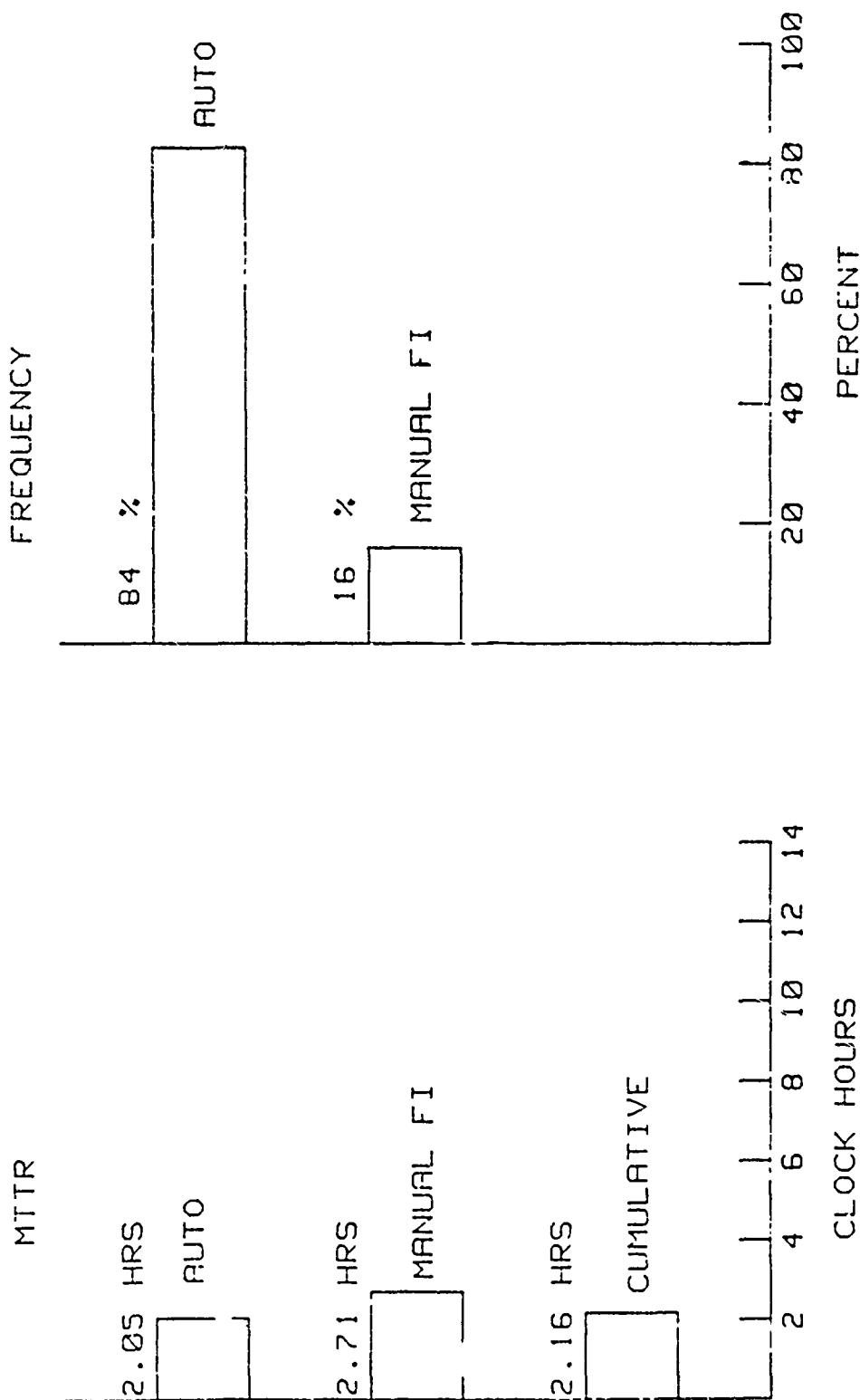


Figure 3-27

FLT-CONT ST/BIT FAULT DETECT/FAULT ISOLATE MTTR ANALYSIS

JAN 1979 - JUN 1980

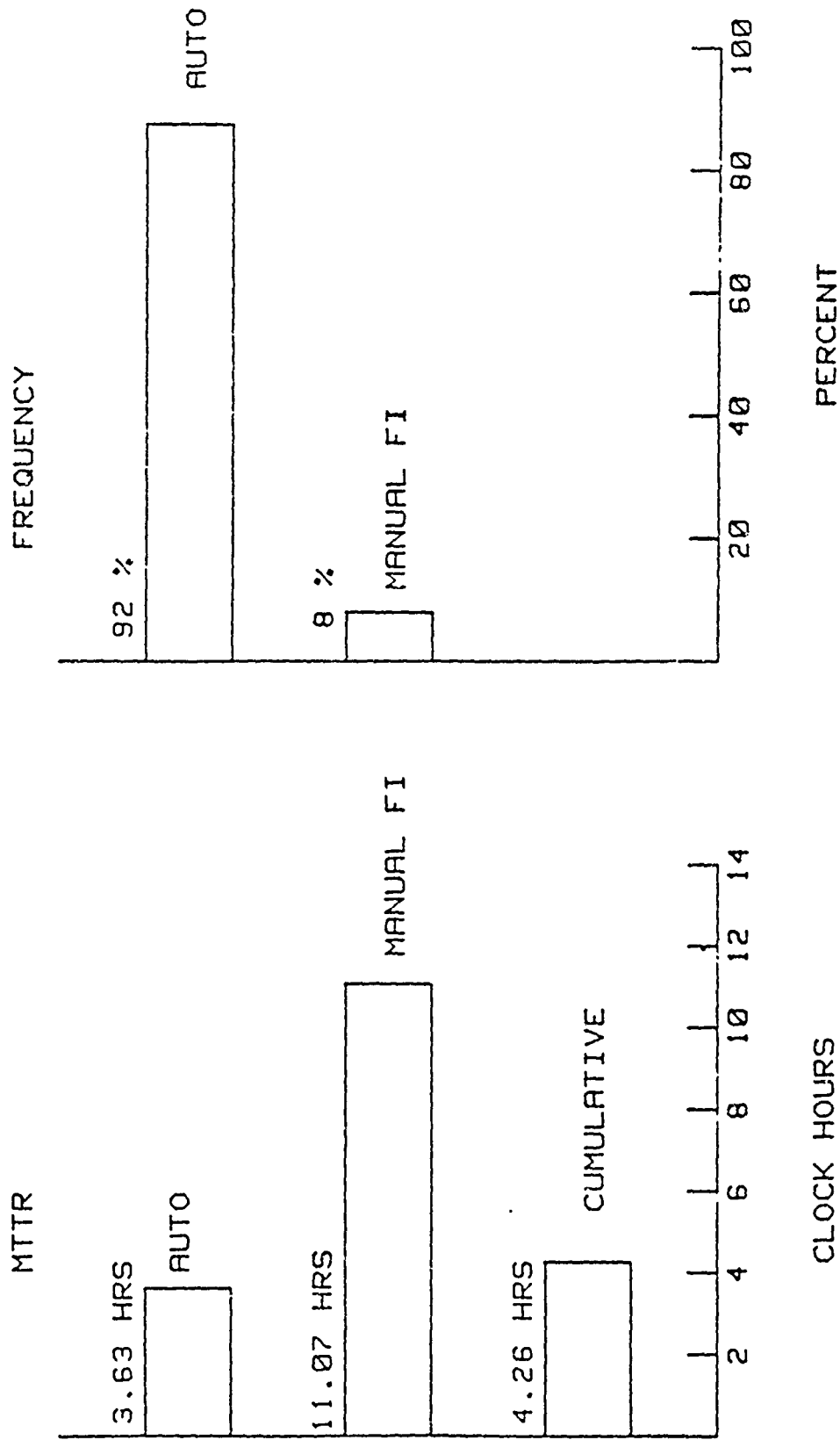


Figure 3-28

F-16 SELF TEST/BIT IMPLEMENTATION
AND
LESSONS LEARNED

Gordon England
GENERAL DYNAMICS, FORT WORTH DIVISION

Mr. England is the Director
of Avionics Systems for the
Fort Worth Division of
General Dynamics

HIGHLIGHTS OF THE PRESENTATION

The presentation covers four specific areas: F-16 avionic descriptions and ST/BIT requirements; F-16 ST/BIT design approach and application of previous lessons learned; F-16 ST/BIT results; and application to future programs.

F-16 capabilities are shown in Figure 4-1; F-16 ST/BIT requirements are shown in 4-2. General overall requirements are specified for the system and then specific subsystem requirements are specified. Since the flight control computer is quad redundant and monitors all failures, no quantitative ST/BIT requirement was stated.

Requirements imposed by General Dynamics on suppliers are shown in Figure 4-3; they are seen to be "stiffer" than those imposed by the Air Force in terms of detection and isolating to FLUs. In addition, General Dynamics has imposed additional requirements of isolating to failed functions within FLUs, which has resulted in about 400 different faults being reported rather than just the total number of LRUs. This secondary fault reporting was imposed by GD on the suppliers. Identification of functional failures permits the pilot to evaluate the effect of a failure on the weapon system.

Figure 4-4 shows the approach taken by GD to establish a total integrated ST/BIT program for the F-16. This program was based on inputs from a number of agencies such as The RAND Corporation and AFTEC, and based on a number of earlier systems

such as the F-15 and the F-111. Each item of the program will be discussed in detail. All items of the F-16 ST/BIT design approach are considered essential to a successful ST/BIT program.

It is important to state at this point that it is essential that one individual be assigned ST/BIT responsibility. This assures a completely coordinated fault detection and isolation development resulting in a good operational capability. Also a single point responsibility will result in a well organized/well managed effort to meet established goals.

The most deliberate front end item requirement is partitioning the system properly to incorporate ST/BIT, as shown in Figures 4-5 and 4-6. The philosophy is that subsystems are self-contained and perform total functions, outputting whole values (not delta values) under the overall control of the FCC. The FCC is a 32 K word machine, of which 27 K words are presently used. Simple interfacing was also considered essential, as indicated in Figure 4-7. For example, the (approximately) 70 wires between the radar and display in the F-111 were reduced to 11 in the F-16. One universal multiplex data line was used for system communication. All symbology is generated within the display based on commands from the FCC.

A stable configuration was considered essential and established as shown in Figure 4-8; primarily because numerous changes can impact the effectiveness of ST/BIT and partly because changes required coordination with all EPG countries. This stability allowed ST/BIT to be incorporated in block changes.

ST/BIT was integrated into subsystems as shown in Figure 4-9. No printers or hardcopy readouts are provided so as to not introduce another item subject to failure. For post flight debriefing and maintenance, the operator writes down the alphanumeric code describing the failure from the FC Navigational

Panel. Most of the systems are operating continuously and are continually monitoring themselves, minimizing the amount of interruptive BIT required.

Early testing was utilized as shown in Figure 4-10. All ST/BIT failure indications were tracked for accuracy of reporting during laboratory and flight tests. Any ST/BIT anomalies were corrected during the development phase. The avionics equipment bay includes a nose section of the aircraft and is tied to a software development facility (dynamic test station) to provide an integrated system to permit formal testing before demonstration in the aircraft. Algorithm deficiencies (e.g., negative velocities in the INS on the ramp) have been detected by this method, eliminating possible numerous CNDs on the NAV Computer. Tech orders are oriented toward field usage, including using T.O. writers in actual maintenance as shown in Figure 4-11.

ST/BIT failures are reported as to function failed, time of failure, and intermittency as shown in Figure 4-12. At the present time, this information is not fully utilized by the AIS, since procedures are not adapted to its use. Takeoff and landing times are also recorded. Proper use of these data (second tier) in the AIS could likely reduce initial test time by 50 percent or more. The AIS development lagged the avionics in order to let it mature, but did not take advantage of secondary fault data.

Data and test requirements were integrated into the design process as shown in Figure 4-13; verification is required throughout the program, using ST/BIT as shown in Figure 4-14.

ST/BIT results at the subcontractor level are shown in Figure 4-15. The same induced faults were also tested with the AIS. Everything reasonable in ST/BIT was done to achieve 95 percent FD/FI without doing anything ridiculous to achieve a specific percentage. An estimate of 10 percent additional

cost for ST/BIT appears reasonable for acquisition costs. The difficulties in early measurement of ST/BIT field data are shown in Figure 4-16. The data base consisted of an 18-month time frame, 22 aircraft, 2899 sorties/3816 flight hours, and 2918 write-ups. ST/BIT results in the field are shown in Figures 4-17 and 4-18. (The total of the "engineering deficiencies" and "no trials" in Figure 4-17 corresponds to the "special category" data of the RADC presentation.) CND rates shown in Figure 4-17 are misleading since they do not consider high reliability items. However, CNDs reduce user confidence. The Suitability Team (Figure 4-19) is useful in determining the specific action required to correct the deficiencies and mature the BIT.

ST/BIT general lessons learned are shown in Figures 4-20. Specification requirements recommended are shown in Figure 4-21. False alarms should be eliminated and not permitted in the specification; threshold and anomaly duration criteria should be set such that momentary faults due to power transients, for example, are not recorded as faults but at the same time record real faults that affect system performance. CNDs and RETOKs should also be eliminated ultimately.

The advantages of implementing BIT at the subsystem level are shown in Figure 4-22; details of the type of data readouts are shown in Figure 4-23. The importance of emphasizing management and control and of incorporating ST/BIT as a first line requirement early in the design of a system are shown in Figure 4-24. Demonstration and test requirements are shown in Figure 4-25. Intermittents can be addressed by use of storage and history provisions as indicated in Figure 4-26. Recommendations for field support and evaluation are shown in Figure 4-27. T.O.s should be prepared by personnel with "hands-on" experience who participate in the initial system integration activities and continue through flight test on the

development hardware to ensure maximum knowledge of systems, features, handling peculiarities and general eccentricities. Training simulators that use the real hardware can now be implemented owing to extensive digital systems that are software intensive, as shown in Figure 4-28. BIT can be correlated with fault isolation at other maintenance levels as shown in Figure 4-29. The design lessons for subsystem BIT are given in Figure 4-30.

A summary of the F-16 experience is given in Figure 4-31. The F-16 has shown the highest sortie rate in the Air Force, used less spares than projected, and achieved both in a relatively short period of time.

DISCUSSION POINTS

- A development program requires a test and evaluation effort similar to that performed by AFTEC on the F-16 in order to be successful. This is one of the most important lessons learned from the F-16.
- The question is whether a program such as the AFTEC F-16 test program, is affordable on all programs; this is in view of the fact that the Air Force has approximately 90 major programs and 200 minor programs in progress at the present time. However, it was pointed out that the F-16 Suitability Team involved only a few people in the field whose inputs were fed directly to the GD engineers at Fort Worth, permitting rapid corrective action. Consequently, considerable benefits were achieved with relatively low up-front investment. The F-16 Suitability Team plans to recommend to TAC that the activities of the Team be continued at the present level rather than be curtailed (as is currently planned).
- Externally generated BIT is more difficult to implement than ST conducted within each subsystem partly because of the numerous Class-2 changes. The inertial system on the F-111 had 13,000 Class-2 changes.
- The inertial navigation system includes 10 percent of its piece parts for self test; however, because of ST-BIT, 95 percent FD/FI is achieved at reasonable cost.
- ST is incorporated in sensor encoders (RIUs) in the F-16. This minimized fault isolation procedures.

- GFE sometimes presents a problem in terms of testing and reporting its own condition and the condition of its sensors.
- Design problems may manifest themselves as a number of different faults. High skill engineers are required to identify problems such as these.
- Fault-tolerant systems have been investigated by General Dynamics in an IR&D program (which is about to become a government-funded program). It includes small, standard throw-away modules with no I-level maintenance, implementing the entire avionics system with eight standard modules.
- Access to faults stored in non-volatile memory should be achieved at 0-level (preferably without powering up the aircraft) and at I-level.
- Maintainability demonstration requires stabilized hardware and software and cannot be moved to an early phase in the program.
- RIWs were used with suppliers to provide incentives for achieving reliability of their subsystems.
- FEMAs are a design tool, providing a discipline for ST/BIT.
- No formal "sneak circuit" analyses were performed. It is of questionable testability value because of the dynamic nature of the systems.
- It is estimated that two to three years are required in the field in order to mature the ST/BIT. Part of this time is related to the quality of the design, the suitability of the failure data, and the ECP process. Changes were approximately 75 percent software and 25 percent hardware. Software changes were sometimes used to correct hardware deficiencies.
- Some airlines are now specifying MTBRs in order to address the CND problem.
- The airlines are also finding that two years are required to mature new avionics systems.
- Nuisance warnings are a problem with the airlines, especially in ground proximity warning systems.
- There was a significant level of discussion on the issue of where there is such a characteristic as a "false alarm" and where a "false alarm rate" should be included in specifications. On one hand it was argued test any time there is an indication of failure to the operator, there is a need to correct some aspect of either the system or the BIT logic, and

therefore there is no such thing as a false alarm. On the other hand, it was argued there are certain transients that occur which cause failure indications but which cannot be completely eliminated. Therefore some minimum false alarm level has to be specified. A consensus was not reached.

Figure 4-1

F-16 AVIONIC SYSTEM CAPABILITIES

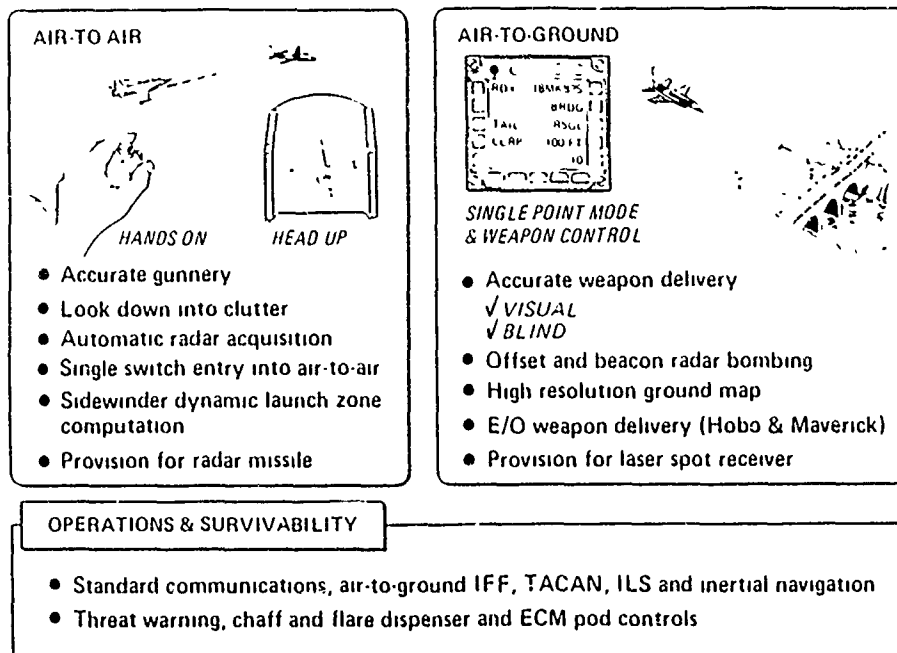


Figure 4-2

F-16 SELF TEST/BUILT-IN-TEST (ST/BIT) REQUIREMENTS

- GENERAL REQUIREMENTS 16PS001 SYSTEM SPECIFICATION
 - REMOVE AND REPLACE AIRCRAFT EQUIPMENT WITHOUT NEED FOR ADJUSTMENT EXCEPT AS PROVIDED BY BIT CAPABILITY
 - MINIMIZE REQUIREMENT FOR FLIGHT LINE SERVICE FOR AVIONICS
 - MAXIMIZE USE OF ST/BIT FOR AVIONICS SYSTEM CHECKOUT AND FAULT ISOLATION
- SPECIFIC REQUIREMENTS 16PS002 AIR VEHICLE SPECIFICATION
 - FIRE CONTROL RADAR - DETECT AND ISOLATE TO LRU FOR 95% OF MALFUNCTIONS
FALSE ALARM (FA) < 1%
 - HUD SET - DETECT CERTAIN FAILURES IN HUD AND 90% OF FAILURES IN SYMBOL GENERATOR < 1% FA
 - FIRE CONTROL COMPUTER - DETECT AND REPORT 95% OF MALFUNCTIONS
 - E/O DISPLAY - DETECT CERTAIN FAILURES IN DISPLAY AND 95% OF FAILURES IN SG/EU < 1% FA
 - INERTIAL NAV SET - DETECT 95% OF FAILURES, ISOLATE 95% OF DETECTED FAILURES < 1% FA
 - FLIGHT CONTROL COMPUTER - INTEGRATED OPERATIONAL CHECKOUT AS PART OF SYSTEM DESIGN - NO QUANTITATIVE ST/BIT REQUIREMENT

Figure 4-3

SUBCONTRACTOR ORGANIZATIONAL LEVEL TEST REQUIREMENTS

SUBCONTRACTOR	ITEM	REQUIREMENT
WESTINGHOUSE	Fire Control Radar	95% Failure Detection 95% Isolation to FLU
MARCONI ELLIOTT	HUD Set	95% Failure Detection 95% Isolation to FLU
DELCO	Fire Control Computer	95% Failure Detection 95% Isolation to FLU
GD	SMS	95% Failure Detection 95% Isolation to FLU
KAISER	E/O Display Set	95% Failure Detection 95% Isolation to FLU
SINGER KEARFOTT	Inertial Nav Set	95% Failure Detection 95% Isolation to FLU
GD/LEAR SIEGLER	Flight Control	Detailed Self Test Design Requirements Specified in Vendor Spec and in Teaming Arrangement. Quad Redundant System Monitors All Abnormalities

Figure 4-4

F-16 ST/BIT DESIGN APPROACH & PREVIOUS LESSONS APPLIED

THE FOLLOWING ELEMENTS WERE IDENTIFIED AS ESSENTIAL TO ACHIEVE A GOOD FAULT DETECTION AND ISOLATION CAPABILITY AT THE ORGANIZATIONAL LEVEL

- A SYSTEMS APPROACH
- A MATURE EQUIPMENT SUITE
- SIMPLE INTERFACES
- STABLE CONFIGURATION
- BIT INTEGRATED INTO SUBSYSTEM DESIGN
- EARLY TESTING OF DETECTION AND ISOLATION CAPABILITY
- ADEQUATE FAULT ISOLATION PROCEDURES (T.O.s) FOR AIRCREW AND MAINTENANCE PERSONNEL
- ADDED FAULT DATA FOR SHOP PERSONNEL
- MANAGEMENT EMPHASIS
- MEANINGFUL DATA AND TEST REQUIREMENTS
- VERIFICATION TESTING
- FIELD SUITABILITY TEAM

Figure 4-5

F-16 AVIONIC SYSTEM PARTITIONED FOR MAINTENANCE

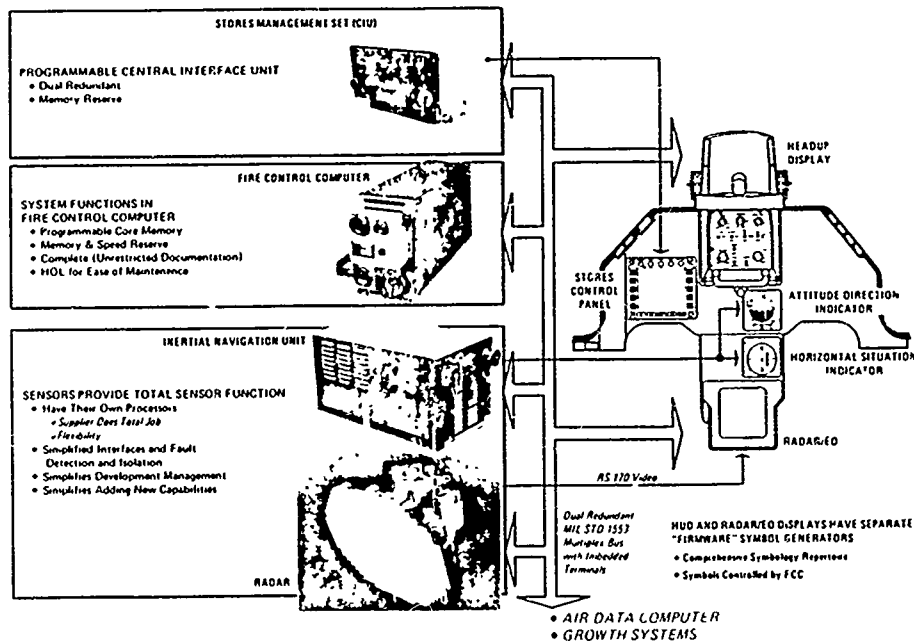


Figure 4-6

DESIGN SIMPLICITY AND MATURITY

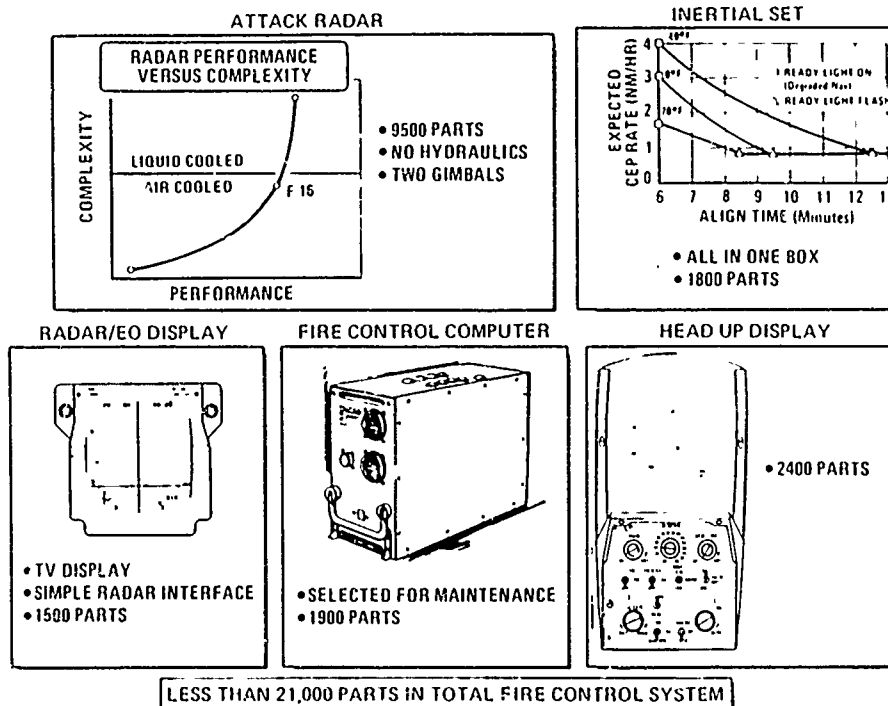


Figure 4-7

SIMPLE INTERFACES

- SYSTEM STRUCTURE RESULTS IN SIMPLIFIED INTERFACE

- DISTRIBUTED PROCESSORS ELIMINATE COMPLEX CROSSTALK
- SCAN CONVERTER IN RADAR REDUCES INTERFACE BETWEEN RADAR AND DISPLAY (Only 11 Wires in F-16)
- ONE BOX INU RESULTS IN CAL DATA, FAILURE DATA AND MOST INTERFACES ALL WITHIN ONE FLU
- SYMBOLOGY GENERATION WITHIN EO DISPLAY AND WITHIN HUD; HENCE, NO CONSTRUCTION SIGNALS IN INTERFACES
- MIL-STD-1553 MUX RESULTS IN ONE UNIVERSAL DATA LINE

Figure 4-8

REASONABLY STABLE CONFIGURATION ESSENTIAL

- PRIOR PROGRAMS SUFFERED FROM NUMEROUS CHANGES TO THE AVIONIC SYSTEMS
 - CHANGES TO BOXES IMPACTED BIT AND INVALIDATED PRIOR M-DEMO RESULTS
 - INADEQUATE FIELD PROCEDURES RESULTED FROM TIME LAGS IN INCORPORATING CHANGE RELATED DATA
 - MAINTENANCE PERSONNEL EXPERIENCED NEGATIVE LEARNING CURVES
 - CHANGES DEGRADED RELIABILITY
- BOTH GD AND THE GOVERNMENT ON THE F-16 WERE COMMITTED TO KEEP CHANGES TO A MINIMUM
 - EPG PARTICIPATING REDUCED CHANGE LEVEL
 - BLOCK POINTS FOR CHANGE INCORPORATION

Figure 4-9

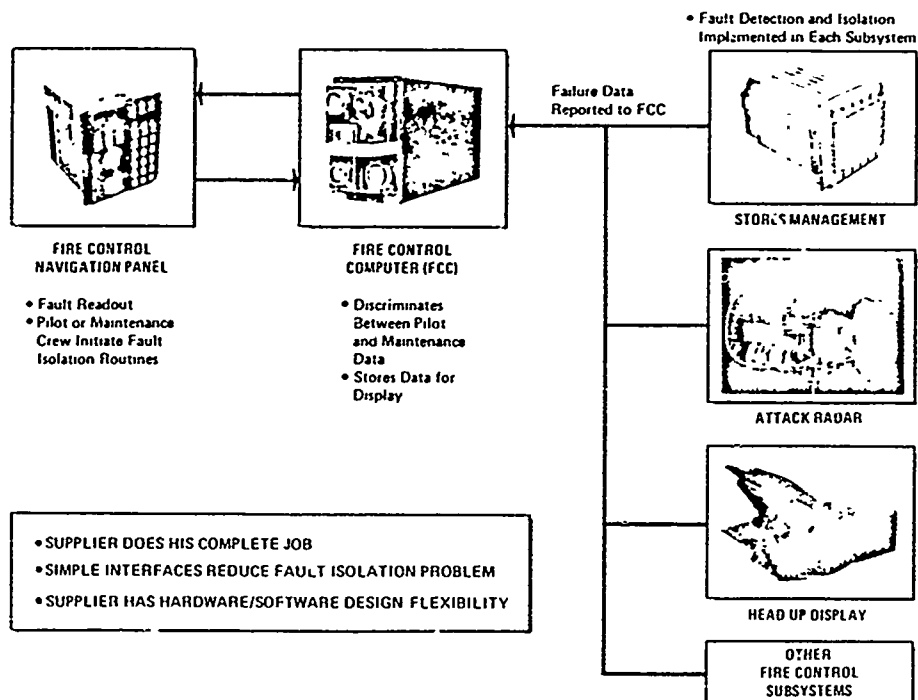


Figure 4-10

EARLY TESTING

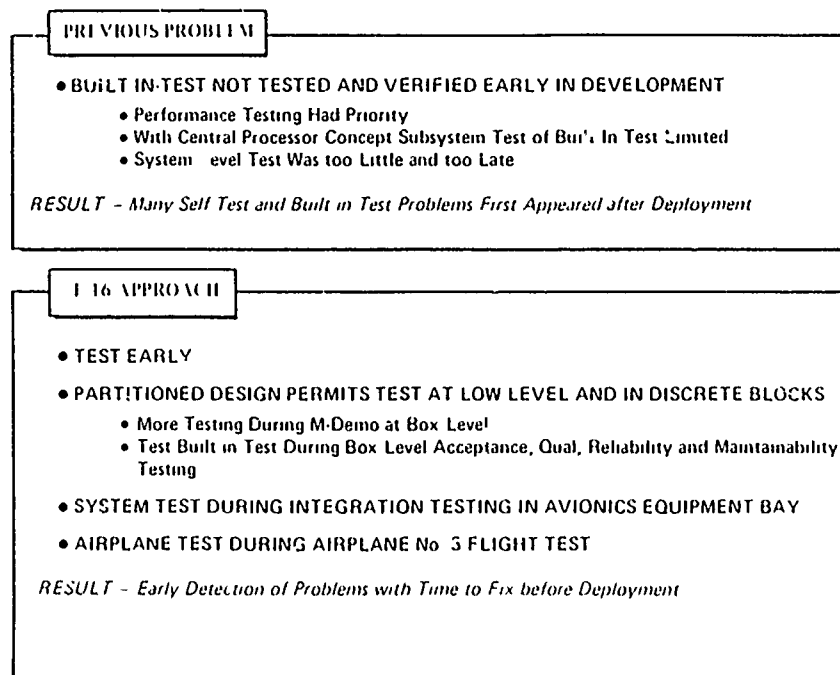


Figure 4-11

NEW T.O. DEVELOPMENT APPROACH

PREVIOUS PROBLEM

- ENGINEERING DEVELOPED PROCEDURES WERE FACTORY RATHER THAN FIELD ORIENTED
- TECH WRITERS PARTICIPATED AFTER INTEGRATION AND LAB TEST COMPLETE
- LIMITED "IN-SERVICE" USE TO VALIDATE TECH ORDERS BEFORE DEPLOYMENT

*RESULT - Inadequate Procedures in the Field
- Equipment Removals and Retest OK's*

I-16 APPROACH

- USE T.O.s IN THE PLANT - NOT MANUFACTURING TEST PROCEDURES
 - ✓ Engineering and Tech Writers to Jointly Develop T.O.s
 - ✓ T.O.s to Be Used During Lab Integration and Early Flight Test
 - ✓ Organization Level T.O.s to Be Released on Airplane No 3 for Validation

RESULT - Usable T.O.s for USAF Operational Support

Figure 4-12

DESIGN SENSITIVE TO AIS NEEDS

PREVIOUS PROBLEM

- DATA REPORTED TO CENTRAL COMPUTER LIMITED TO GO NO GO
 - ✓ Shop Personnel Had No Data Relevant to Failure Mode
 - ✓ Intermittent Failures Not Captured

*RESULT - Numerous Retest OK's
Difficult Fault Isolation in Shop*

I-16 APPROACH

- INTERNAL SUBSYSTEM FAULT DATA IS REPORTED TO FCC
 - ✓ Failure Functions Within Each FLU Are Reported
 - ✓ Failures Tagged by Mission Phase and Time

*RESULT - Shop Has Detail Failure Data to Zero in on Bad Part
Odds Improved in Finding Intermittents*

Figure 4-13

DATA AND TEST REQUIREMENTS STRENGTHENED

PREVIOUS PROBLEM

- DATA REQUIREMENTS GENERALLY LIMITED TO BROAD MAINTENANCE CONCEPTS AND PLANS
- VERIFICATION OF BUILT IN TEST LIMITED TO 10-15 INDUCED FAULTS IN M DEMO

*RESULT Built in Test Evolved with No Analytical Basis
Low Confidence in M Demo Results*

F-16 APPROACH

- DATA ITEMS KEYED TO BUILT IN TEST
 - ✓ Failure Mode and Effects Analysis (FMEA) to Identify Failures by Built in Test
 - ✓ Quantitative Analysis of Built in Test Required
 - ✓ Self Test and Built in Test Control Document for Radar
- MEANINGFUL M DEMO REQUIRED, SUPPLEMENTED BY SUBSYSTEM TESTING
 - ✓ 50 Induced Faults, 150 for Radar

*RESULT Data Items Focus Attention to Built in Test, Provides Better Visibility Early
Early Testing More Meaningful*

Figure 4-14

VERIFICATION TESTING

ST/BIT AN INTEGRAL PART OF SYSTEM AND SUBSYSTEM TESTS

• SUBCONTRACTOR – SUBSYSTEM LEVEL

- Module Build Up Testing
- LRU Testing, Engr Evaluation, Qual, M-Demo
- Formal Acceptance Testing

• CONTRACTOR – SYSTEM LEVEL

- Hardware Integration – with Other Avionic Systems
- Software Development – Operational System Mode Development
- Avionics Equipment Bay – Flight Simulation
- FSD Flight Test

Figure 4-15

SUBCONTRACTOR ORGANIZATIONAL LEVEL TEST RESULTS

SUBCONTRACTOR	ITEM	GEN DYNAMICS REQUIREMENT	SUBCONTRACTOR INITIAL PREDICTION	RESULT
Westinghouse	Fire Control Radar	95% Failure Detection 95% Isolation to FLU	> 95% > 97%	94% Failure Detection 95% Isolation to FLU
Marconi Elliott	HUD Set	95% Failure Detection 95% Isolation to FLU	> 95% > 95%	94% Failure Detection* 95% Isolation to FLU
Delco	Fire Control Computer	95% Failure Detection 95% Isolation to FLU	98% 98%	95% Failure Detection 95% Isolation to FLU
GD	SMS	95% Failure Detection 95% Isolation to FLU	In Work	95% Failure Detection 95% Isolation to FLU
Kaiser	E/O Display Set	95% Failure Detection 95% Isolation to FLU	95% 95%	94% Failure Detection* 95% Isolation to FLU
Singer Kearfott	Inertial Nav Set	95% Failure Detection 95% Isolation to FLU	> 95% > 95%	95% Failure Detection 95% Isolation to FLU
GD/Lear Siegler	Fight Control	• Detailed Self-Test De- Sign Requir'ts Specified in Vendor Spec and in: Teaming Arrangement, Quad Redundant System Monitors All Abnormalities	NA	95% Failure Detection 95% Isolation to FLU *Bit (Visual) Used to Supplement ST to Achieve 94% Detection

Figure 4-16

EARLY MEASUREMENT OF FIELD/OPERATIONAL LEVEL IS VERY DIFFICULT

- ONE OR TWO SUBTLE DESIGN PROBLEMS CAN APPEAR TO BE GROSS
ST/BIT PROBLEMS
- ✓ RAW DATA NOT RELEVANT
- CAN'T SEPARATE INTERMITTENTS AND CNDs FROM DATA BASE
- EARLY INEXPERIENCE/IMMATURITY OF PERSONNEL AND
SUPPORT EQUIPMENT APPEAR AS ST/BIT PROBLEMS

COMPREHENSIVE DATA NEEDED WITH ON SITE
SKILLED ENGINEERS TO DRAW VALID CONCLUSIONS

Figure 4-17

SUMMARY OF EARLY USAF EVALUATION OF F-16 ST/BIT

ENGINEERING DEFICIENCIES (1211)	<ul style="list-style-type: none"> • EARLY RADAR PRODUCED A GREAT NUMBER OF FAULT INDICATIONS WHICH WERE NOT DUPLICABLE <ul style="list-style-type: none"> ✓ "New Radar Self test Mechanization Allows These Faults to Be Isolated" • SMS "BLANKING" PROBLEM • MISSILE SLAVING FUNCTION SELF TEST DESIGN DEFICIENCY CORRECTED AT BLOCK 10
NO TRIALS (685)	<ul style="list-style-type: none"> • MAINTENANCE MADE NO ATTEMPT TO WORK WRITE UP <ul style="list-style-type: none"> ✓ SMS and Radar Major Contributors ✓ SMS - Assigned to Wrong Career Field ✓ Radar - Primarily Intermittent Faults
CND'S (466)	<ul style="list-style-type: none"> • FURTHER EVALUATION NEEDED
ADDRESSABLES (556)	<ul style="list-style-type: none"> • 93% OF FAULTS AUTOMATICALLY DETECTED • 92% OF DETECTED FAULTS ISOLATED TO CORRECT LRU

Figure 4-18

DETAILED UNDERSTANDING OF DATA YIELD DIFFERENT RESULTS

(CND EXAMPLE)

SUBSYSTEM	RAW ST/BIT CND RATE	SOURCE OF CND	ACTUAL ST/BIT CND RATE
FIRE CONTROL COMPUTER	65%	62% Confirmed as Several FCC OFP Problems Since Corrected 3% (1 Unit) Insufficient Data to Analyze	3%
HEAD UP DISPLAY SET	79%	54% Due to Only Two Identified Self Test Design Inconsistencies 13% Due to 1 Intermittent EU (Hardware Failure) 5% Due to Other A/C System	7%
RADAR/EO DISPLAY SET	67%	30% Due to Unique MOT&E Class II Mods 20% Due to MFLs 001 & 008 - Under Active Investigation 17% One Time Occurrences (July 79 - Jan 80) on 5 Different A/C and Have Not Repeated	0 - 17%
INERTIAL NAVIGATION SET	22%	14% Due to Recycling of INS Power in Less than 1 Minute - Violates Procedure 6% Intermittent Failing Hardware Likely 1% Confirmed Intermittent Failure	1 - 6%
FIRE CONTROL RADAR	34%	4% S/T Timing Problem - Fix in Later Config 9% Turn On Bit Problem 2% Test Mech Problem - Fix in Later Config 4% S/T A/D Circuit Checks - Fixed in Later Config 10% Unknown	15%

WITH DETAILED UNDERSTANDING OF DATA A PROPER PERSPECTIVE AND APPROPRIATE CORRECTIVE ACTION CAN BE TAKEN

Figure 4-19

SUITABILITY TEAM

- FLIGHT TEST
 - TRACK, ANALYZE AND TAKE CORRECTIVE ACTION ON EVERY SELF-TEST/
BIT REPORT
- F-16 DEPLOYMENT
 - MANAGEABLE SAMPLE SIZE FOR TRACKING AND DETAILED FOLLOW THROUGH
 - SUITABILITY TEAM
 - Contractor and USAF
 - Complete and Accurate Data Base
 - On-Site Follow Through
 - Common Data Base
 - "Qual" Type Accelerated Data (MOT&E)
 - SUPPLEMENT SUITABILITY TEAM DATA WITH AIS AND DEPOT CND/RTOK
MONTHLY REPORTS

Figure 4-20

GENERAL SYSTEM LESSONS

- MAXIMIZE NON-INTERRUPTIVE TEST
 - SIMPLIFIES SYSTEM OPERATION
 - MINIMIZES OPERATOR INTERACTION
- STORE AND REPORT ALL FAILURE DATA
 - MAY PERMIT SRU IDENTIFICATION DIRECTLY
- KEEP VISUAL FAULT DETECTION REQUIREMENTS TO A MINIMUM
- SUBSYSTEM READY DISCRETE
 - SUBSYSTEM HAS POWER APPLIED
 - ENOUGH TIME ELAPSED FOR ALL BITS AT THE MUX INTERFACE
TO BE CREDIBLE

Figure 4-21

SPECIFICATIONS

- BIT FAULT DETECTION AND ISOLATION REQUIREMENTS ARE REASONABLE AND ACHIEVABLE IN THE 95% RANGE
- FALSE ALARM REQUIREMENTS RELATIVE TO BIT SHOULD BE CHANGED FROM 1% TO NO FALSE ALARMS – NOT MEANINGFUL AND CAN'T BE MEASURED

NOTE Intermittent Failures Are Not Considered False Alarms

- MAINTAINABILITY DEMONSTRATIONS, QUAL TESTS AND ACCEPTANCE TESTS SHOULD BE TIED TO BIT REQUIREMENTS; i.e., BIT SHOULD BE USED AS A PRIMARY INDICATION OF FAILURES DURING DEMONSTRATIONS

Figure 4-22

SYSTEM-VS-SUBSYSTEM BIT

- BIT FOR A GIVEN SUBSYSTEM SHOULD BE TOTALLY SELF CONTAINED WITHIN THAT SUBSYSTEM, MORE SPECIFICALLY WITHIN INDIVIDUAL LRU
 - SUBSYSTEM MANUFACTURER HAS TOTAL RESPONSIBILITY AND CONTROL OF HIS DESIGN
 - HIGHER ORDER TESTS OR OTHER SUBSYSTEMS HAVE LIMITED VISIBILITY INTO INDIVIDUAL LRUs
- DEPENDENCE ON PROPER PERFORMANCE OF OTHER SUBSYSTEMS LEADS TO INCORRECT FAULT ISOLATION

Figure 4-23

PILOT-VS-MAINTENANCE CREW FAULT DATA READOUT

- TO SIMPLIFY THE PILOT'S TASKS OF INTERPRETING FAULT DATA, FAULTS REPORTED TO THE PILOT SHOULD BE ALPHABETIC DESCRIPTIONS INSTEAD OF CODED MESSAGES.
- MAINTENANCE CREWS TYPICALLY HAVE TIME TO DECODE MESSAGES AND CODED FAULT REPORTS
- FAULT DATA CAN BE USEFUL TO THE PILOT TO ASCERTAIN WEAPON SYSTEM CAPABILITY

Figure 4-24

MANAGEMENT AND CONTROL

MANAGEMENT EMPHASIS IS ESSENTIAL

- THE CONTRACTING AGENCY, THE CONTRACTOR AND SUBCONTRACTOR MUST RECOGNIZE ST/BIT AS A LEGITIMATE FIRST LINE REQUIREMENT WITH THE SAME LEVEL OF IMPORTANCE GIVEN PERFORMANCE REQUIREMENTS

EARLY DESIGN EMPHASIS

- TOTAL SYSTEM DESIGN MUST BE COORDINATED EARLY WITH INDIVIDUAL SUB-CONTRACTORS TO ASSURE COMPATIBILITY OF DESIGNS
- DESIGN ENGINEERS MUST BE COMMITTED TO DESIGNING TESTABLE EQUIPMENT EARLY
- ST/BIT DESIGN ANALYSES MUST BE PERFORMED EARLY; PRIOR TO COMMITTING DESIGN TO HARDWARE
- DESIGN SHOULD CONTAIN THE MAXIMUM AMOUNT OF FLEXIBILITY TO ACCOMMODATE DEVELOPMENT CHANGES

Figure 4-25

DEMONSTRATIONS AND TEST

- ST/BIT SHOULD BE AN INTEGRAL PART OF SYSTEM, SUBSYSTEM AND LRU TESTING
- INTEGRATION TESTS SHOULD CONTAIN SPECIFIC ST/BIT OBJECTIVES
- MAINTAINABILITY DEMONSTRATIONS SHOULD BE DESIGNED AROUND ST/BIT
- LRU TESTING, QUALIFICATION AND BENCH TESTS SHOULD CONFIRM ST/BIT FUNCTION
- PERHAPS A SPECIAL ST/BIT TEST SHOULD BE PERFORMED INDUCING AT LEAST ONE TYPE OF EACH TYPICAL FAULT WITHIN AN LRU
- INTERMEDIATE LEVEL TESTS SHOULD CONFIRM ST/BIT RESULTS
- FIELD FOLLOW-UP A MUST – ALL POSSIBLE CONDITIONS AND EVENTS IN THE FIELD ARE EXTREMELY DIFFICULT TO PREDICT AND EACH INDIVIDUAL EVENT MUST BE TRACKED. FIELD EXPERIENCE AND SYSTEM MATURITY GO HAND-IN-HAND

Figure 4-26

INTERMITTENTS

- INTERMITTENT FAILURE CONDITIONS ARE GENERALLY DIFFICULT TO ISOLATE
- ST/BIT SYSTEMS WITH STORAGE AND HISTORY PROVISIONS PROVIDE VALUABLE INSIGHT INTO LOCALIZING AND ISOLATING INTERMITTENT FAILURE OF LRUs IN THE SHOP
- SUCH STORAGE SHOULD BE A SPECIFICATION REQUIREMENT

Figure 4-27

FIELD SUPPORT AND EVALUATION

THE BEST DESIGN EFFORT COUPLED WITH EXTENSIVE ANALYSES STILL DO NOT INSURE 100% PERFORMANCE WHEN SYSTEMS ARE DEPLOYED. THERE IS A MATURATION PROCESS THAT ACCOMPANIES THE DEVELOPMENT OF AVIONIC SYSTEMS. SYSTEM COMPLEXITY AND NEW TECHNOLOGIES NECESSITATE A MATURATION PERIOD FOR BOTH FSD AND PRODUCTION PHASES

- FIELD TEAMS

- Experienced Systems Engineers On-Site to Evaluate Events and Assess System Performance

- DATA COLLECTION AND FOLLOW-UP

- Personnel On-Site to Collect Data Are Necessary
- Personnel Assigned to Follow-Up Problem Areas and Effect a Solution

Figure 4-28

TRAINING SIMULATORS

- WITH THE EXTENSIVE USE OF MICROPROCESSORS IN HARDWARE, CHANGES TO SYSTEMS (ECPs) CAN BE HANDLED TO A LARGE EXTENT BY SOFTWARE CHANGES
- MAINTENANCE TRAINING IN THE USE OF ST/BIT DOES NOT REQUIRE EXTENSIVE SIMULATIONS OF ALL FLIGHT PARAMETERS AND A/C ATTITUDES REQUIRED BY SIMULATION SYSTEMS
- USE OF THE ACTUAL AVIONIC HARDWARE CAN BE MORE EFFECTIVE AND ECONOMICAL

Figure 4-29

BIT CORRELATION TO OTHER TEST LEVELS

- TEST RESULTS AT THE A/C CAN PROVIDE VALUABLE FAULT INFORMATION FOR FAULT ISOLATION IN THE SHOP
- TEST TIMES CAN BE REDUCED BY ENTERING TEST PROGRAMS AT POINTS THAT CORRESPOND TO FUNCTIONAL FAILURES
- INTERMITTENT FAULTS, HAVING BEEN DETECTED BY BIT, CAN BE CONCENTRATED ON IN THE SHOP
- BIT CAN BE USED IN THE SHOP TO VERIFY CORRECTIVE ACTIONS
- TREND DATA CAN BE ACCUMULATED IN THE SHOP TO LOCATE BAD ACTORS OR OVERALL FLEET PROBLEMS
- THE AIR FORCE SHOULD IMPLEMENT PROCEDURES TO MAKE FLIGHT LINE DATA AVAILABLE TO THE SHOPS

Figure 4-30

SUBSYSTEM DESIGN LESSONS

- SUBSYSTEM VENDORS SHOULD PERFORM SUBSYSTEM FAULT ANALYSIS AND TESTING TO PROVIDE INFORMATION REGARDING SYSTEM DEGRADATION ASSOCIATED WITH EACH FAULT INDICATION
- A SUBSYSTEM SELF TEST DESIGN SHOULD KEEP THE SEQUENCE OF TESTS INDEPENDENT OF THE SUBSYSTEM MODE TO THE EXTENT POSSIBLE. THIS FEATURE IS DESIRABLE SINCE IT KEEPS THE LIMITATIONS OF MODE SELECTION FROM INHIBITING THE PERFORMANCE MONITORING OF ANY TESTS
- WHILE DEVELOPING A SUBSYSTEM'S SELF TEST CAPABILITIES, AN ANALYSIS SHOULD BE MADE EARLY IN THE DESIGN TO DETERMINE THE INTERDEPENDENCE OF TESTS. SHOULD THE DESIGN REQUIRE A DEGREE OF INTERDEPENDENCE BETWEEN TESTS, A HIERARCHY SHOULD BE ESTABLISHED TO DETERMINE THE ORDER OF THE INDIVIDUAL TESTS.
- WHERE APPLICABLE, THE SAME FAULT INFORMATION WHICH IS TRANSMITTED TO THE CENTRAL COMPUTER/STORAGE DEVICE SHOULD BE STORED WITHIN A SUBSYSTEM'S NON VOLATILE MEMORY

Figure 4-31

SUMMARY

- F-16 DESIGN EMPHASIZED ST/BIT
 - FIELD PERFORMANCE IS GOOD
- MANY INNOVATIVE FEATURES WERE INCORPORATED INTO F-16 ST/BIT DESIGN
 - APPLICABLE TO OTHER PROGRAMS
- F-16 LESSONS LEARNED PROVIDE BASELINE FOR FUTURE SYSTEM SPECIFICATION AND DESIGN

F-16 AN/APG-66
ST/BIT SUCCESS STORY

Jim Victor
WESTINGHOUSE

Mr. Victor is the manager of maintainability, BIT, and safety engineering for Westinghouse, DESC.

HIGHLIGHTS OF THE PRESENTATION

The capabilities of the F-16 AN/APG radar system are seen in both the Air-to-Air and Air-to-Surface modes. In the Air-to-Air mode these include downlook detection; uplook detection; ACM/dogfight autoacquisition; manual acquisition; and range, angle and velocity track. In the Air-to-Surface mode these include real beam ground map; expanded map; Doppler beam-sharpened map; air-to-ground ranging; sea target detection; beacon; and freeze. AN/APG-66 operating features include: head-up, hands-on critical switchology; long-range all-aspect detection and track; clean scope display/downlook target detection; low target false alarm rate; good inherent raid resolution; multiple autoacquisition modes; comprehensive multimode ECCM; high resolution ground mapping/target designation; sea clutter rejection for ship detection; accurate AGR inputs to fire control computer for weapon delivery; high reliability/availability; and comprehensive ST/BIT.

Terminology and modes of operation for the F-16 radar ST/BIT are shown in Figure 5-1. Ease of access of subunits is emphasized in ST/BIT. Self test is defined as fault detection; BIT is defined as fault isolation.

The AN/APG-66 ST/BIT maintenance concepts and specification requirements are shown in Figures 5-2, 5-3 and 5-4. The mechanization of ST/BIT on the radar system is shown in Figure

5-5. Figure 5-6 displays a simplified block diagram and 5-7 displays the F-16 A/C readouts of ST/BIT results.

The management approach to ST/BIT is shown in Figure 5-8, and 5-9 displays the central role of the maintainability/engineer manager. Overall program milestones are shown in Figure 5-10, and Figures 5-11 through 5-16 display the ST/BIT maintainability milestones. Figure 5-11 is a condensed overview of the major milestones; 5-12 through 5-16 is a breakout of these major points. Figure 5-17 presents the in-house testing and demonstration schedule on the F-16 radar system, and Figure 5-18 breaks down the maintainability growth plan for the system. Maintainability trade-offs are shown in Figures 5-19 through 5-22. The growth of self-test/built-in-test experience with the F-16 is shown in Figure 5-23. Block 4 was isolated and elaborated on in Figure 5-24. Software modifications are shown; there are 10 software break-ins in this block, thereby reducing the number of hardware changes required. The computer has 34 K words of memory, of which 4 K are used for self test. A total of 108 key parameters were identified as being required for ST/BIT to be 100 percent complete. Completion included programming, debugging and verifying the parameter test.

Pre-demo faults were inserted for the internal use of Westinghouse as shown in Figure 5-25 to give confidence to a successful demonstration. The number of faults inserted were related to the expected failure rates of the units. The total number of SRUs was 79.

The results of the 0-level maintainability demonstration are shown in Figure 5-26. ST/BIT production improvements for the F-16 radar are demonstrated in Figure 5-27. Figure 5-28 shows the data analysis and corrective action approach agreed to by an evaluation committee which provided for the recognition of problems and the implementation of correction action

in the field. The committee helped to fill the gap between the spec requirements (which had been met) and the user requirements. The program for improving the ST/BIT was part of the overall AFTEC test program and was not costed separately. Block B (flying in the MOT&E aircraft) problems are identified in Figures 5-29 and 5-30. The corrective actions taken to Block B problems as implemented in ECP-331 are shown in Figures 5-31 and 5-32. Snowy runways and squat switch bounce problems were pointed out, including their effects on calibration routines. New APG-66 ST/BIT mechanizations in ECP-331 are indicated in Figure 5-33. The comparison in supportability between the Block B and ECP-331 configurations shows that in some cases the aircraft flew multiple missions with the same fault because maintenance was deferred to the end of the day.

Results and conclusions of MOT&E data analysis on ECP-331 configured aircraft are shown in Figures 5-34 and 5-35 indicating that some faults not confirmed by BIT may indicate trends in system degradation. Figures 5-36 and 5-37 delineate F-16 lessons learned; it is noted that the levels of fault detection for pilots and maintenance should be treated differently since their requirements are different. Development plan requirements are shown in Figure 5-38; operational development requirements are shown in Figure 5-39.

Looking to the future, the essential steps necessary to successfully fulfill ST/BIT requirements are shown in Figure 5-40; recommendations for an effective BIT program are given in Figures 5-41 through 5-49.

DISCUSSION POINTS

- Inconsistencies have been shown between pilot reports and 0-level maintenance tests as well as between successive 0-level maintenance tests. BIT software is an integral part of the operational software.

- Airlines' experience is that 15 percent of the shop failures are "hard" failures (e.g. opens and shorts). It was questioned whether the BIT is mechanized to detect "soft" (e.g. timing) failures and intermit-tents. Westinghouse stated that it has set parameter sensing levels to sense soft failures.
- Trend data indicating unit deterioration and projected need for replacement are not recognized by the avionics maintenance and supply system at the present time. We should investigate the use of this trend data.
- "Beyond BIT" maintenance requires a high-skill-level technician.
- The field problem is not the detection of the fault but rather too many false alarms.
- The problem of specifying a MTBR is that removals will be held to a minimum rather than removed as required for the most effective maintenance.
- A measurable definition of "false alarm" is required. In the EF-111, for example, keying of the HF radio resulted in a false alarm that was ultimately worked-around-clearly--a false alarm.

Figure 5-1

Self-Test/Built-In Test Terminology and Modes of Operation

- Self-Test Is a Continuous Noninterruptive Fault Detection Function That Is Mode Oriented
 - CPM: Continuous Performance Monitor
 - NI: Noninterruptive
 - Offbar: Tests Conducted at Antenna Turnaround
- Built-In Test Is a Hierarchical Group of Interruptive Tests That Detect and Isolate Failures to a Single LRU
 - BIT_{Radar}: Automatically Initiated at System Turn-On
 - BIT_{FCC}: Pilot Initiated Via A/C Fire Control Nav Panel

Figure 5-2

F-16 AN/APG-66 O-Level Maintainability Requirements

- Fault Detection $\geq 95\%$
- Fault Isolation $\geq 95\%$
- Maintenance Time
 - Mean (Mct) ≤ 0.5 Hour
 - MAX (Mmaxct) ≤ 1.0 Hour
- $\leq 5\%$ False Alarm
- No Adjustments, Alignments or Calibrations Permitted
- No Flight Line AGE Required
- Within Skill Level Three Capability

Analysts	Test or Demo	Inspection
✓	✓	
✓	✓	
✓	✓	
✓	✓	
	✓	✓
	✓	
	✓	

INTERMEDIATE LEVEL MAINTENANCE CONCEPT Figure 5-3

- LRU MAINTENANCE TIME
 - MEAN (M_{CT}) 1.0 HOUR
 - MAX (M_{MAXCT}) 2.0 HOURS
- AVIONICS INTERMEDIATE TEST STATION (AIS)
 - 97% ISOLATION TO FAULTY SRU
 - REMOVE AND REPLACE FAULTY SRU
 - VERIFY REPAIR OF LRU
- WITHIN SKILL LEVEL FIVE CAPABILITY
- FAULTY SRU FORWARDED TO DEPOT FOR REPAIR

DEPOT LEVEL MAINTENANCE CONCEPT Figure 5-4

- SRU FAULT ISOLATION REQUIREMENTS
 - SINGLE ELEMENT 80%
 - TWO ELEMENTS 85%
 - THREE ELEMENTS 90%
- DEPOT TEST STATION
 - ISOLATION TO COMPONENT
 - REMOVE AND REPLACE FAULTY COMPONENT
 - VERIFY REPAIR OF SRU
- REPAIRED SRU RETURNED TO STORES

Figure 5-5

Self-Test Built-In-Test Mechanization

- Self-Test is Used to Determine the Health Status of the Radar
 - Self-Test Report (6002) to the FCC Is a Single Bit Report
 - Single Self-Test Fault (6002) Report Can Be Set as a Function of as Many as 80 Different Checks
 - No Means Exists for Determining Which Self-Test Check Failed
- Built-In-Test Is a Fault Isolation Routine that Is Interruptive and Isolates a Failure to an LRU
 - Automatic at Initial Turn-On
 - Pilot Initiated Whenever Derived

The diagram illustrates the architecture of the F-16 Avionics Mux Bus Analog to SMS (AIM-9L) system. The central component is the **Computer**, which is connected to the **Processor** via a **DSP Bus**. The **Computer** has sections for **P.S. CPU**, **a/c Inter**, **Missile Inter**, **I/O Mem**, and **I/O**. It receives **dc Inputs** and **Synchro Inputs** and outputs **Analog to SMS (AIM-9L)**. The **Processor** includes **P.S.**, **Synchronizer**, **I/O**, **Proc**, **Scan**, and **Conv**. It outputs **RS-170 Video**. The **Transmitter** has sections for **TWT**, **Pulser**, **H V**, **P S**, **I Protection & Confid**, **I/O**, and **LVPS**. The **LPRF** (Low Power Radar Frequency) has sections for **Controller**, **Stato**, **Rec**, **Video & A/D Conv**, and **P S**. The **RCP** (Range Control Processor) has sections for **Power Supply**, **Mode**, **Range**, **Freq**, **Pri**, and **Antenna Scan**. The **Antenna** has sections for **P S**, **Uniphase Driver**, and **Servo**. The **Digibus** connects the **Computer**, **Processor**, **Transmitter**, **LPRF**, and **RCP**. The **I-Q Bus** connects the **Processor**, **LPRF**, and **RCP**. The **Triggers & Timing** signal is sent from the **Processor** to the **Transmitter** and **LPRF**. The **Antenna** is connected to the **Transmitter** and **LPRF** via a circulator.

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F-16 A/C Readout of ST/BIT Results

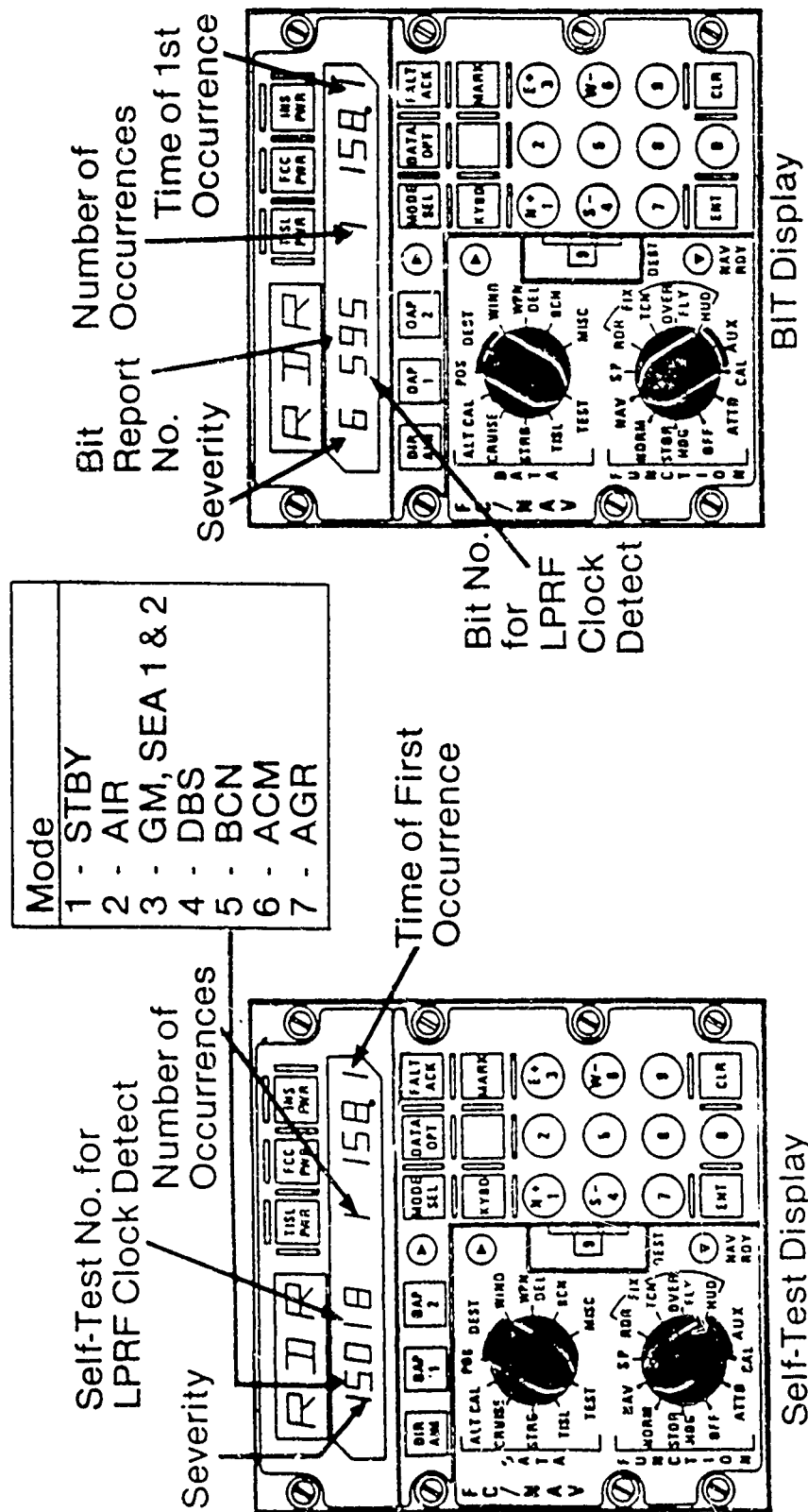


Figure 5-7

Figure 5-8
ST/BIT/M Organizational Interface

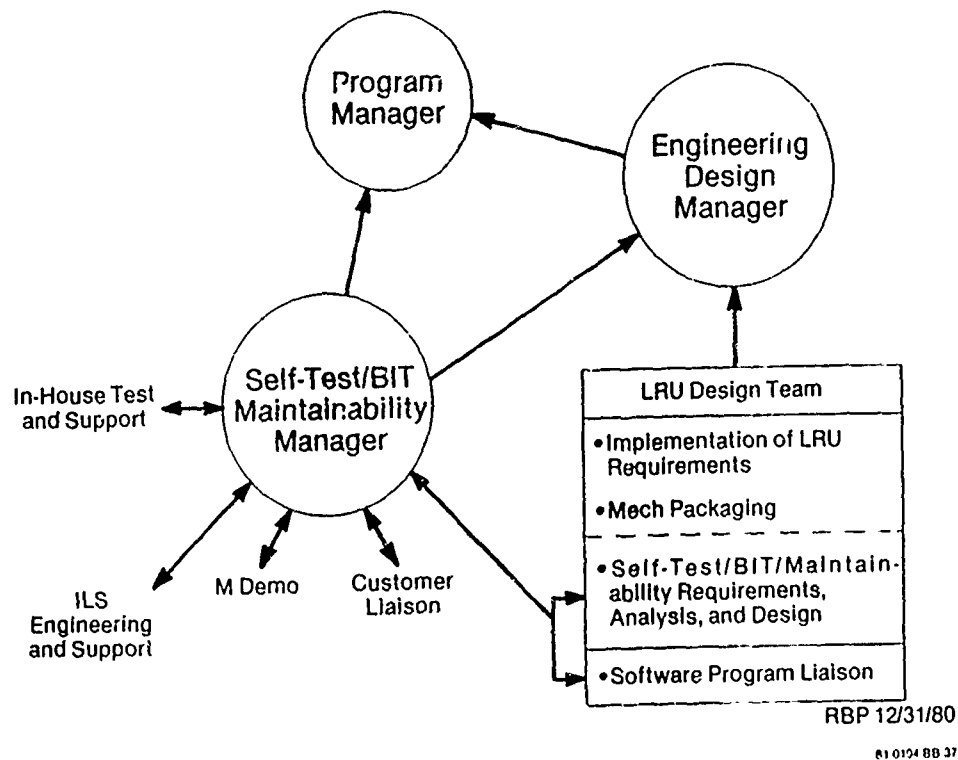


Figure 5-9
S.T./BIT/M Engineer Role

- Member of Design Team
- Specializes in Maintainability Requirements
- Relieves Designer of Added Maintainability Design Functions
- Maintainability Engineer Available for:
 - Impromptu Discussions/Reviews
 - Trade-Offs
 - LRU Partitioning
 - Raw Engineering Data Early
(Parts List, Schematics, T-Specs, etc)
 - Drawing Sign-Off

Program Milestones

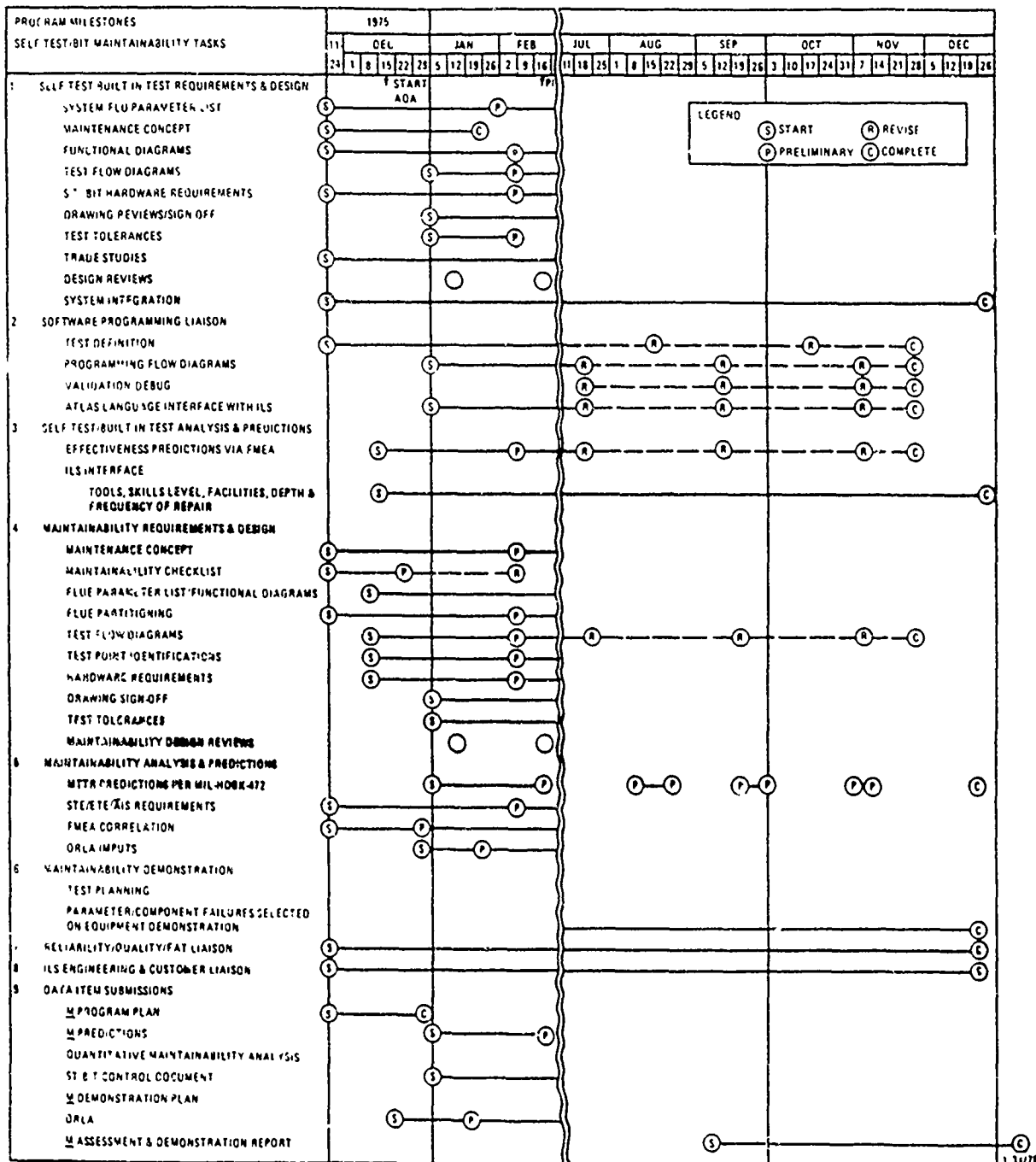
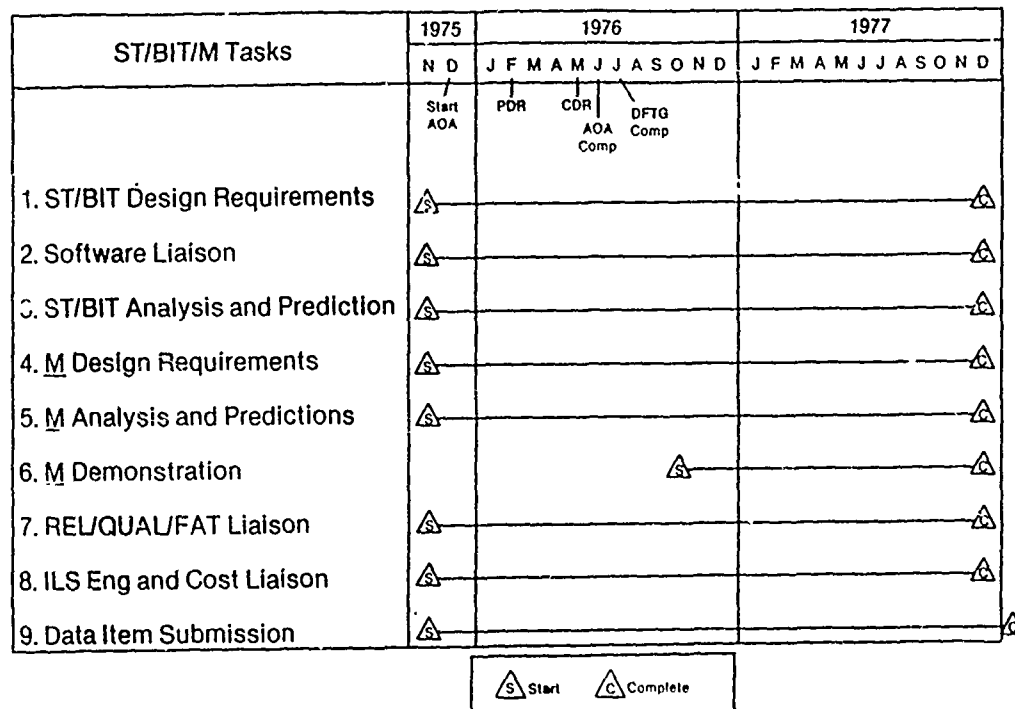


Figure 5-10

81-G-04-BB-23

Figure 5-11

Self-Test/BIT/Maintainability Milestones



810104 RB 24

Figure 5-12

Self-Test/BIT/Maintainability Milestones

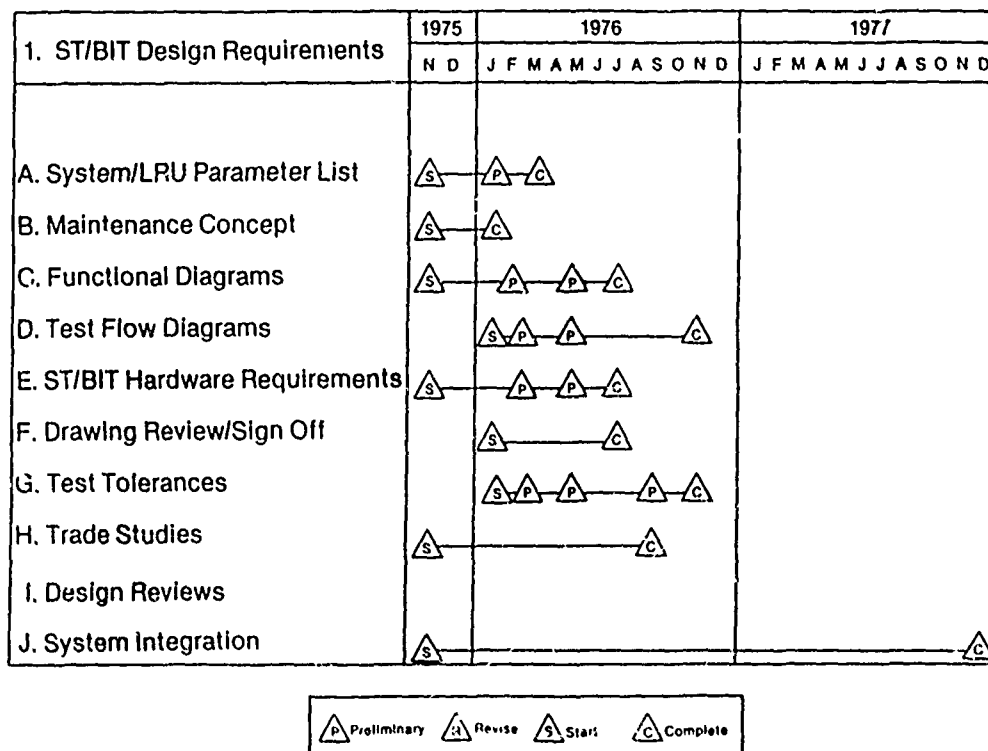


Figure 5-13
Self-Test/BIT/Maintainability Milestones

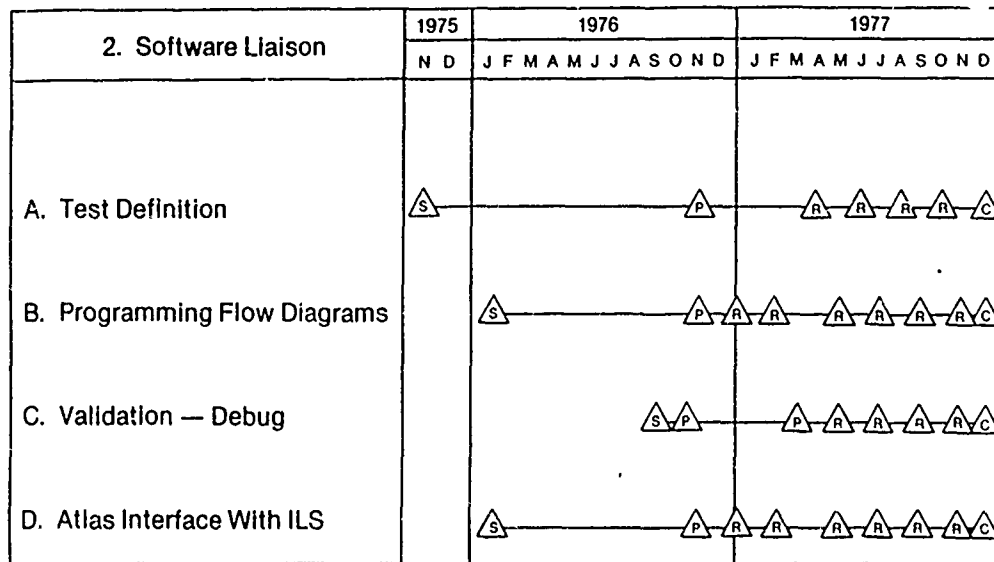


Figure 5-14
Self-Test/BIT/Maintainability Milestones

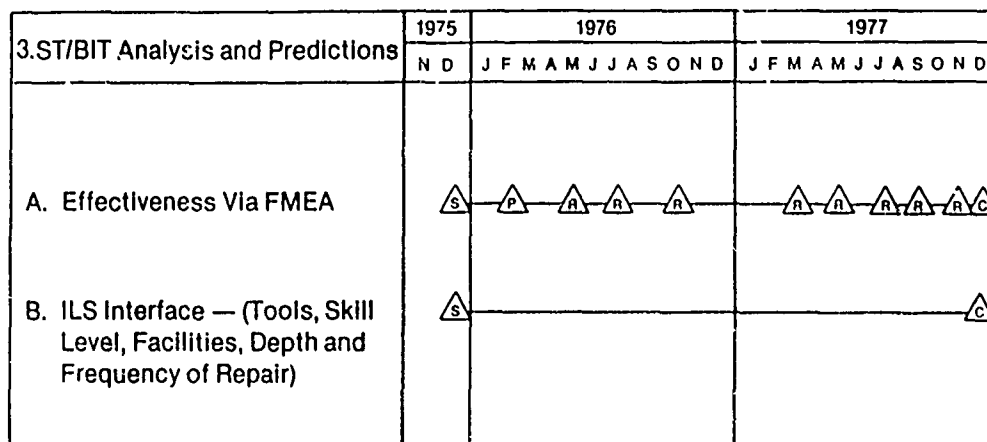


Figure 5-15
Self-Test/BIT/Maintainability Milestones

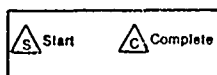
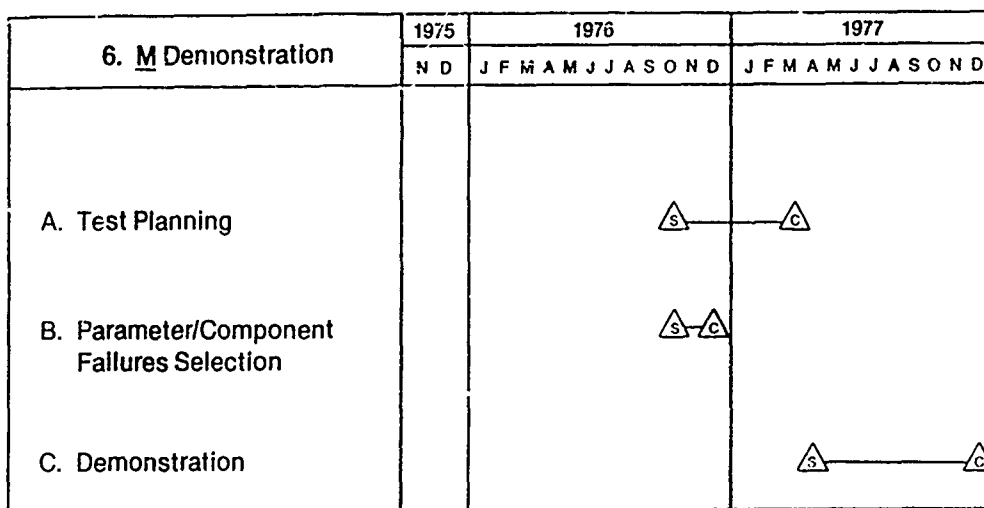


Figure 5-16
Self-Test/BIT/Maintainability Milestones

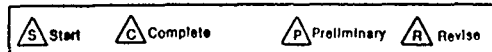
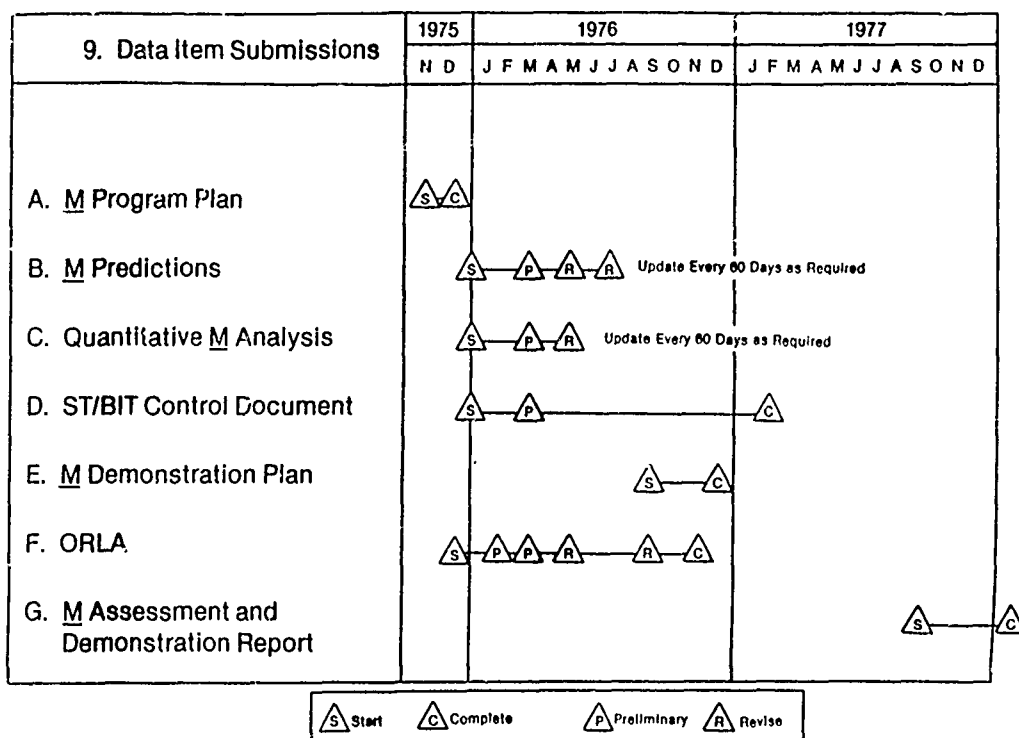


Figure 5-17

S.T./BIT/M In-House Testing and M Demonstration Schedule

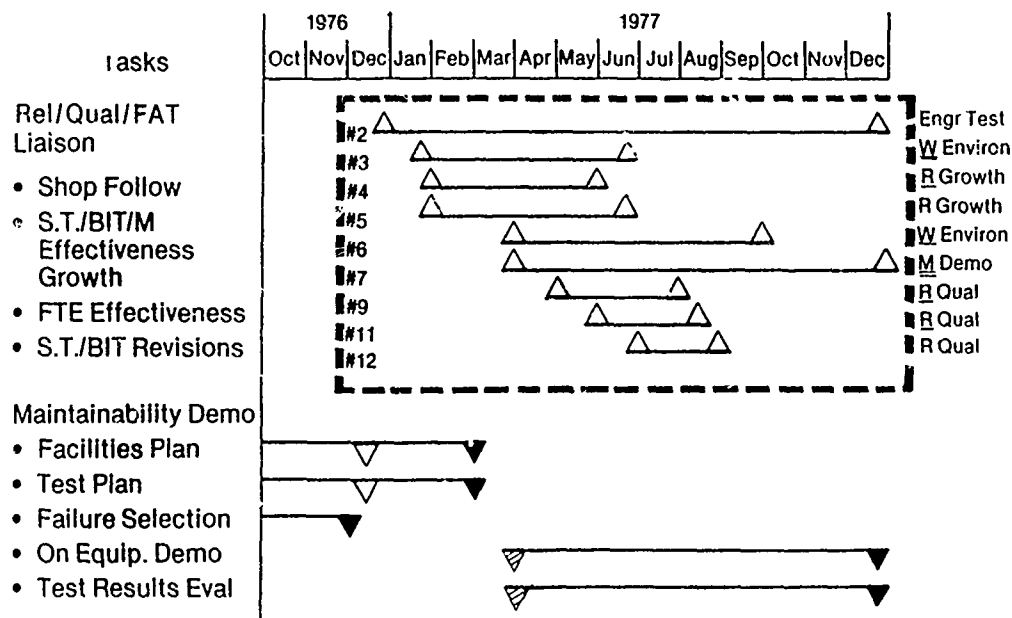


Figure 5-18

Maintainability Growth Plan

- ≈ 45 Months of System Test Time at Westinghouse
Excluding Factory Acceptance Test
- NMR Includes S.T./BIT/M Data
- S.T./BIT/M Effectiveness Data Collected Via Tape Recorded
Telecon
- Above Reporting Provides:
 - Large Data Base
 - Repair/Retest Concept Implemented Early in FSD
 - Measured Effectivity of: STE/ETE
ATS
STS
S.T./BIT/M

Figure 5-19

Maintainability Trade-Offs

- STALO Multiplier SRU
- Pressurization System
 - LVPS Distribution
 - RCP BIT Board Elimination

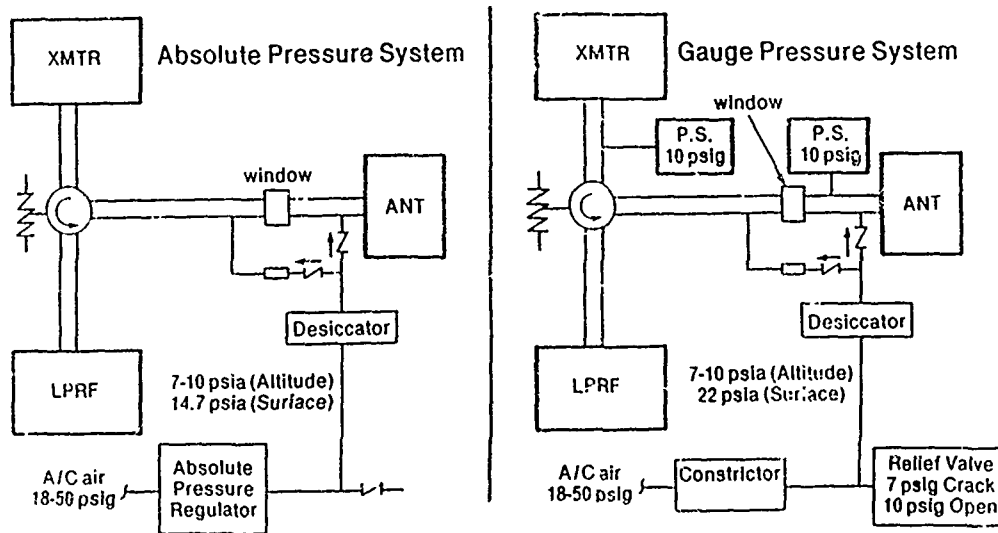
Figure 5-20

Waveguide Pressurization Trade Study

<u>Absolute Pressure System</u>		<u>Gauge Pressure System</u>	
<u>Cost</u>	\$620 Life Cycle Cost Savings \$160	<u>Permits</u>	On-Ground Self-Test/BIT When
<u>Reliability</u>	Less Average Seal Stress (0 to 10 psia * vs 7 to 10 psia * *)	• A/C Engine Air (Servo Air)	
		or	
		• AGE (Pressurization Bottle)	
		Is Provided.	
<u>Size</u>	117 cu in. Smaller (84 vs 201 cu in.)		
<u>Weight</u>	0.5 lbs Lighter (3.3 lbs vs 3.8 lbs)		
	* Only at High Altitudes * * All Altitudes		

81-0104 RB 11

Figure 5-21
Waveguide Pressurization

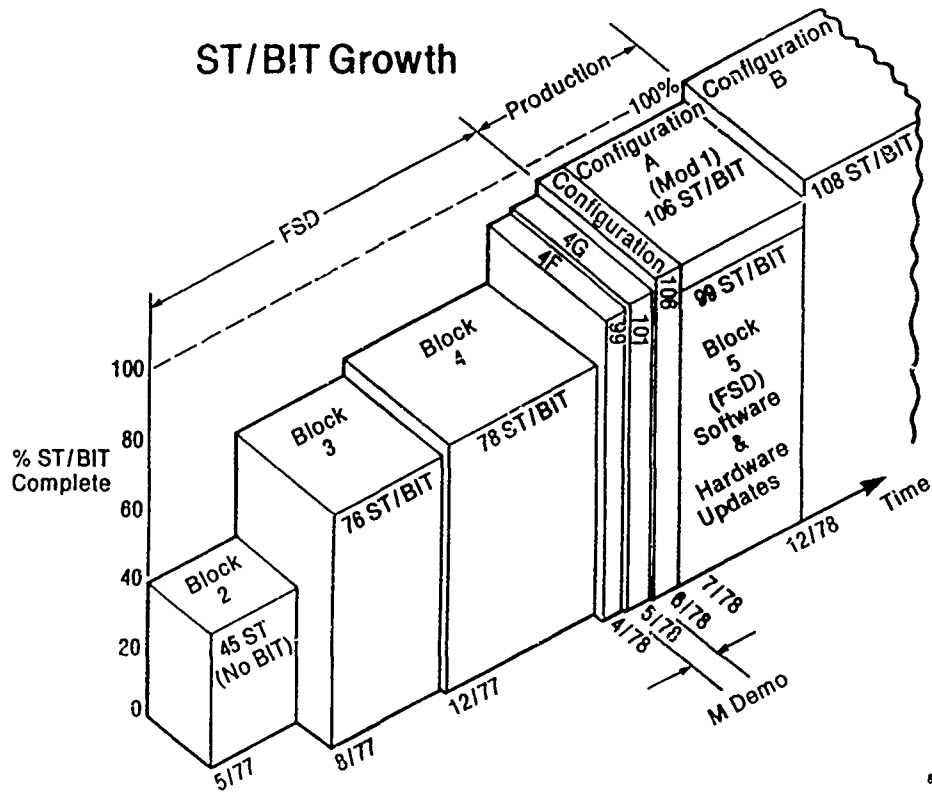


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Figure 5-22
Distributed LVPS Trade Study Summary

- Reduces Built-In-Test Complexity
- Improves Maintainability Through Easier Troubleshooting
- Reduces Factory and AGE Test Equipment Complexity and Cost
- Reduces LRU Interconnection Cabling and Cable Wiring Protection
- One Less LRU To Be Maintained, Handled, and Spared
- Reduces Interface and Harmonization Problems at System Level
- Reduces Weight, Component Count (By 7%), and Cost

Figure 5-23



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Figure 5-24

FSD Software Modifications & Block Update Summary

Configuration BIP	System Performance Patches	ST/BIT Patches
Block 4A	157 Patches	42 Patches
Block 4B	31 Patches	9 Patches
Block 4C	25 Patches	7 Patches
Block 4D	17 Patches	9 Patches
Block 4E	85 Patches	34 Patches
Block 4F	16 Patches	10 Patches
Block 4G	0 Patches	3 Patches
Block 4H	32 Patches	6 Patches
Block 4I	35 Patches	11 Patches
Block 4J	7 Patches	3 Patches
Subtotal 405		Subtotal 134
Total 539		

Figure 5-25

Pre-Demo Fault Insertion Status

	No. of SRUs Faulted	Faults Detected Faults Inserted	No. of Tests Exercised
Antenna	5	54/56	13
LPRF	11	80/120	30
Transmitter	8	27/33	14
DSP	27	958/1090	19
Computer	13	86/103	17
RCP	3	43/60	6
Total	67	$\frac{1248}{1462} = 85\%$	99

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Figure 5-26

F-16 FCR O-Level Maintainability Demonstration Requirements and Results

- Maintainability Demonstration Requirements
 - 150 Faults To Be Inserted Throughout Six LRUs and Distributed According to Relative Failure Rates (Selected Via Random Number Generator)
 - Each SRU (79 Total) Shall Have at Least One Failure Inserted
- Maintainability Demonstration Results

Self-Test Fault Detection
94%
Built-In-Test Fault Isolation
98%

Figure 5-27

AN/APG-66 Production Improvements

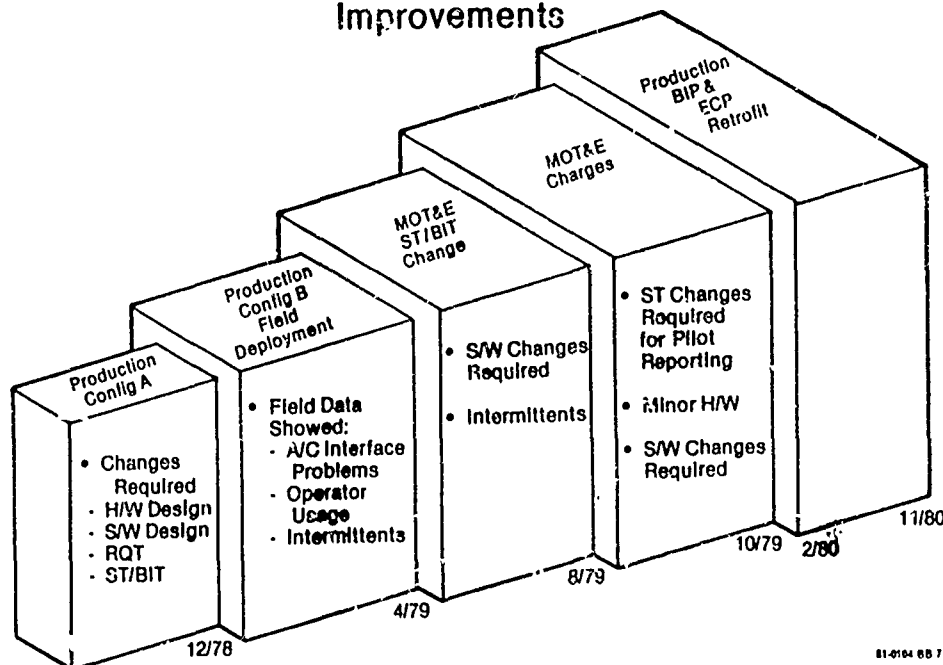


Figure 5-28

**Joint (W)/G.D./USAF
Agreement as a Result
of Meeting at HAFB**

(7-26-79)

- Agreed Upon Approach of Increasing Catastrophic Faults and Labeling Them as 1010 Reports on FCNP.
- Agreed Upon Eliminating 6002 Reports from MCL and Retaining 6002, 1010, BIT Reports and Self-Test Fault Flag Filter in the MFL Recall Function.
- Agreed Upon a Joint (MOT&E, SPO, AFTEC, G.D., (W)) Committee Evaluation of MOT&E Results Periodically.

- Phase I Phase II Phase III

Figure 5-29

What Were the Pilot Noted Problems Affiliated With Self-Test and Built-In Test? (Block B)

- Self-Test Reports Occurred In-Flight Too Often, Illuminated the Master Caution Light, and the Pilot Debrief Report Stated:
 - Frequently the Radar Worked OK
 - Frequently, Can't Run BIT at Time of Self-Test Failure
 - Frequently No Failures Noted When BIT Was Run
 - Conclusion: Self-Test Was of No Value to the Pilot

Figure 5-30

APG-66 ST/BIT Problems Incurred at HAFB With Block B Configuration

- Self-Test Reports Do Not Provide an Indication of Which LRU is Defective
- Frequently Postflight Maintenance Fails to Reproduce In-Flight ST Reports
- Self-Test Problem Created the Following Situations:
 - Pilot Has Little Confidence In Self-Test or Built-In Test
 - Many Maintenance Hours Spent Trying to Duplicate Self-Test/Built-In Test Reports
 - Many CND's and RTOK's Due to "Shot-Gun" Removal of LRU's
- Built-In Test Is Not a Problem
 - LRU's Removed for BIT Report Are Usually Defective

Figure 5-31

APG-66 Improvements in ECP-331 That Correct Block B ST/BIT Problems

- Computer Hardware Changes to Eliminate Hang-Up Condition (1005)
- Antenna Flipper Hardware Change and Retrofit
- System OFP Software Changes That Affect ST/BIT
 - System Calibration Routines Modified To Meet Operational Scenario
 - Transmitter Protection and Control Logic Modified
 - Antenna Overtemperature Logic Modified
 - A/C Interface Modifications
 - Squat Switch Bounce
 - ECS Shutdown
 - INU Down Accounted for
 - DSP Initialization Header Word Fix
 - Computer Hang-Up Restart Logic Modified

Figure 5-32

APG-66 Improvements in ECP-331 That Correct Block B ST/BIT Problems

- ST/BIT Software Corrections and Improvements Summary:
 - Transmitter Peak Detect Failure
 - Transmitter High Voltage Failure
 - Transmitter Calibration Failure
 - MSL 2001 Report
 - Antenna Drive Defective
 - Synchronizer Test Failure
 - TX Peak Detector Failure at TOF/from STBY
 - ST Reports Before Required Warm-up
 - BIT 6450 Reports at Initial Turn-on
 - Transmitter Peak Detect Failure in DBS Mode
 - MSL 2001 Report at Radar Turn-on
 - MSL 2001 Reports During Radar Self-Test
 - Intermittent Receiver Verification Failure
 - Self-Test Failures Not Duplicable on Ground
 - Only Catastrophic Fault Reports Illuminate MCL

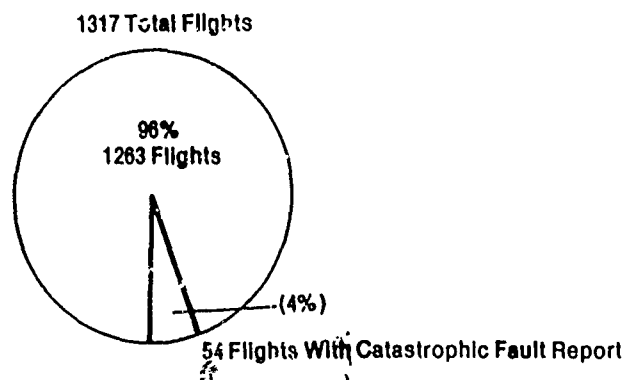
Figure 5-33

Changes Included in ECP-331 Regarding Self-Test Reporting System

- WEC Increased Catastrophic Fault Reports from 4 to 31 Tests
- WEC Provides 6 Words (80 Bits) to the FCC in Self-Test, Indicating the Failed Parameter
- GD Eliminated ST Report (6002) from illuminating the A/C Master Caution Light
- GD Illuminates the Master Caution Light as a Function of Catastrophic Faults, Only (1010)
- MFL Continues to Store 1010's, 6002's, BIT Report Numbers, and the New ST Fault Flag Reports
- New ST Fault Flag Reports Stored in Separate List (RST)

Figure 5-34

Results and Conclusions of MOT & E Data Analysis (3-80 to 12-80)

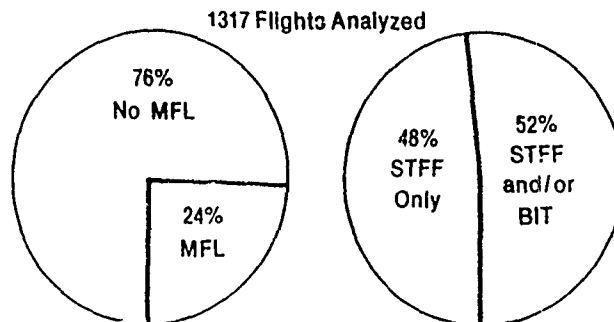


Conclusion:

- Previous Nuisance Indicators of ST Failures Clearly Resolved

Figure 5-35

Results and Conclusion of MOT & E Data (9 A/C from 3/80 thru 12-80)



- Conclusions:
- Worst Case - Only 11.5% of Flights Required STFF Usage
 - Once MFL Report Is Cleared by LRU Removal, Everything Is Super
 - Performance
 - Reliability
 - Availability
 - ST/BIT
 - STFF Is an Early Indicator of System Degradation

Figure 5-36

F-16 AN/APG-66

Specification Lessons Learned

- Maintainability Specification Requirements Should Consider Operational User's Inputs and Needs
 - Pilot Needs
 - Maintenance Technician Needs
- Method of Validating Requirements Should Include Field Operational Usage
 - Requires New Specs
 - Requires Field Dedicated Personnel and Assets and User Organization Similar to AFTEC
- Consideration Should Be Given to Intermittent Malfunctions (Not Duplicatable on Ground) and Effect on Higher Level Maintenance

Figure 5-37

F-16 AN/APG-66 Specification Lessons Learned

- Self-Test/Built-In-Test False Alarm Rate Requires Following:
 - Clear Definition of Same
 - Practical Requirement, Taking Into Consideration Other Parameters Like Fault Detection/Fault Isolation Effectiveness and System Reliability.
 - Practical Method of Verification

Figure 5-38

F-16 AN/APG-66 Development Plan and Lessons Learned

- Comprehensive Detail Planning, Scheduling, and Monitoring Should Include:
 - ST/BIT Development, Integration, and Check-Out Concurrent With System Performance Development
 - Assignment of Personnel and Equipment Assets
 - Pre-Demo and In-House Effectiveness Monitoring
 - : Institute Test/Fix/Retest Program
 - Mil-Std-470 Should Be Revised
- Above Elements Are Necessary Toward Obtaining Operational Requirement But the Task Is Not Yet Complete

Figure 5-39

F-16 AN/APG-66 Operational Development

- **Successful Demonstration of Requirements Is Not Attained Until:**
 - **It Works as Intended With:**
 - A. **User Personnel**
 - B. **User Equipment Assets**
 - C. **User Tech Orders**
 - D. **Actual Environmental Conditions**
 - E. **Actual Operational Scenario**

Figure 5-40

Essential Steps Necessary to Successfully Fulfill ST/BIT Requirements

- **Program and Engineering Management Commitment**
- **ST/BIT/Maintainability Engineers Must Be an Integral Part of Design Team**
- **Detailed ST/BIT Program Plan Development Required To Be Integrated With System Development Program Plan**
- **System Assets Need To Be Committed to ST/BIT Development**
- **Engineering Personnel and Equipment Assets Required for Extended Time Duration After Initial Field Deployment**
- **Joint Plan Involving Contractor, SPO, MOTE, and Tactical Units Required for Data Collection and Field Evaluation**

Figure 5-41

Main Program Elements

- Definitive Specifications
- Effective Contractor Program
- Formal Measure of Achievement
- Field Feedback and Problem Correction

Figure 5-42

Specifications

Fault Detection

- Probability of F D for:
 - : Operational - Expanded Tolerance Limits
e.g., ± 3 dB
 - : Maintenance/Preflight - Minimum Acceptable Limits
e.g., ± 1 dB
- Define Means of Annunciation of a Fault
- Define Class of Faults To Be Reported
 - e.g., Only Hard Faults,
M of N Transient Faults,
All Faults.
- Define Requirement for Data Capture of:
 - : Faults Not Reported During Operation
 - : Operating Conditions at Time of Fault
e.g., Altitude, Temp, Mode, G's, Time, etc

Figure 5-43

Specifications (Continued)

Fault Isolation

- Probability of Unambiguous FI to: 1 LRU
2 LRUs
- Define LRU
 - : Large Box - 3 Level Maintenance
 - : Plug in Assembly - 2 Level Maintenance
 - : Discard Element - 1 Level Maintenance
- Define Beyond BIT Maintenance for Each Assembly

Figure 5-44

Specifications (Continued)

False Alarms

- Define a False Alarm -
(An Intermittent in an Essential Circuit Should Not Be Classified as a False Alarm)
- Express Requirement as False Alarm Rate
e.g., F.A. Shall Not Exceed 0.01/Mission Oper. Hr.
- Define Requirement for Transient Data Capture

Reconfiguration

- Specification Minimum Allowable Probability of Mission Success Which Includes Reconfiguration Effectivity
- Specify Reliability Maturation Status
i.e., What Fraction of Predicted Reliability Value is the Basis for Field Use?

Figure 5-45

Specifications (Continued)

Trade Studies

- Define Criteria - LCC
 - LSC
 - Acquisition Cost

Qualification Test Requirements - See Separate Chart

Data Items

- BIT Program Plan - Submit 90 DAC
- Allocation, Analysis and Assessment Report - Submit 90 DAC Update Quarterly
- BIT Growth Plan - Submit at PDR
- BIT Qualification Plan - Submit 90 DAC
- Final Design Report
- Field Feedback and Corrective Action Plan - Submit at CDR
- Field Effectiveness Report - Quarterly

Figure 5-46

Contractor Program Definition

BIT Program Plan

- Define - Contractors BIT Design Organization
 - Analysis/Prediction Techniques
 - Design Monitoring Process
 - Allocation of Requirements to Subordinate System Elements
 - Allocation of: Resources
 - : Manpower
 - : Prime Equipment Time
 - : Money
 - Milestones
 - Configuration Control - Hardware
 - Software

Figure 5-48

Contractor Program Definition

BIT Growth Plan

Define - Maturation Process

(Recommend Randomly Selected Fault Insertion)

- Resources in a Test/Fix/Test Iteration Process
- Milestones
- Objectives To Be Met
- Corrective Process

Figure 5-48

Formal Measure of Achievement

BIT Qualification Test

- Specify Test Sample Size - Must Be Statistically Significant
- Define Sample Selection Process - Failure Weighted
 - Random Selection
- Define Evaluation Team Personnel
- Specify Pass/Fail Criteria for Each Parameter
- Specify Evaluation Test Process for Such Parameters
 - : False Alarm Rate
 - : Circuit Elements In Which a Simulated Fault Could Be Catastrophic
e.g., A Short on a 90 KV P.S. Could Destroy the Entire Unit
- Define Liability of Contractor if Test Does Not Achieve Minimum Limits

Figure 5-49

Field Feedback and Problem Correction

- Define User/Producer Field Evaluation Team
- Define Evaluation Team Objectives
- Define Team Member Responsibilities
- Define Team Evaluation Criterion
- Define Problem Correction Process
- Define Problem Correction Liability to the Contractor

F/A-18A AND TF/A-18A
AVIONICS BIT

Bob Drummond
McDONNELL DOUGLAS

Mr. Drummond is a Section
Chief, Electronics, at
McDonnell Douglas

HIGHLIGHTS OF THE PRESENTATION

The presentation covered the following six aspects of F/A-18A and TF/A-18A avionics BIT: objectives; integration and design considerations; BIT specification requirements; system description; design-development-verification process; and status. It is noted that the internal mechanization, including BIT, of the fighter (F)/attack (A) aircraft is the same and requires no internal hardware or software changes when reconfiguring between "fighter" and "attack."

The major objectives of avionics BIT are shown in Figure 6-1. In meeting these objectives, the following four results were obtained. Though not a specified requirement, BIT may be run by one person, resulting in additional manpower savings. Organization Level GSE has been eliminated and I-level fault isolation (FI) has been simplified by initiating test in the failed area identified by BIT, rather than initiating a complete subsystem test. Cooling fans automatically initiated during ground maintenance permit ground operation without external support equipment up to 103°F (above that, the system automatically shuts down). BIT code readout of the maintenance monitor panel can be activated using aircraft battery power. In-flight presentation of the weapon system status combined with automatic mode reversions demonstrate the potential for a significant increased mission effectiveness.

A summary of BIT integration and design considerations is shown in Figure 6-2. Off-the-shelf equipment comprises

approximately 35 percent of avionics equipment and requires unique integration interfaces. The BIT failure criteria implemented to minimize false alarms is summarized in Figure 6-3 and includes thresholds and time delays. The operational flight envelope and environment must be considered and experienced in developing these thresholds and delays. In the aircraft, for example, several MUX bus faults in succession on a channel must take place prior to declaring a failure.

The development of BIT thresholds by vendors and MCAIR generally began with developing tight tolerances and then expanding them as guided by in-flight BIT performance results achieved while operating in the operational and environmental conditions, as illustrated in Figure 6-4. There are 41 WRAs which contain BIT in the fighter aircraft configuration and 58 in the attack configuration (with 2 pods). Failures are reported in the cockpit, on the WRAs themselves, and one on the MMP in the nose wheel well. Tolerances for periodic BIT and initiated BIT are the same; however, the initiated BIT employs more extensive tests. Automatic reversion to a degraded mode or manual mode is performed upon declaration of a failure. Selected override (emergency) provisions are included and maintenance indications of the override are retained in memory. Widening BIT tolerance values unjustifiably may make BIT initially look good but will not result in an effective BIT system.

BIT time delay considerations are shown in Figure 6-5, seeking the bottom of the bell curve as an optimum condition.

A summary of the BIT requirements imposed on the aircraft, as well as the requirements imposed on the suppliers, are shown in Figure 6-6. The requirement to detect 98 percent of the equipment failures applies to individual major avionics subsystems. Depending upon the subsystem, periodic BIT is performed every 200 milliseconds to 30 seconds. An initial

analysis was required from each vendor to demonstrate their designs capability to detect 98 percent of the failures.

General F/A-18A status monitoring interfaces are illustrated in Figure 6-7. A total of 19 air-to-ground and 13 air-to-air tactical parameters are monitored for training purposes, as well as certain airframe and engine parameters to measure stress and performance trends. Avionics (NONMUX) equipment BIT interface is via the CSC to the MC and avionic MUX compatible equipments interface directly with the MC. Display to the pilot is in real time; i.e., for an intermittent, the BIT indication will come and go. The maintenance monitor panel in the nose wheel well provides a stored 3 digit BIT code retrievable by ground maintenance personnel.

BIT operating characteristics are shown in Figure 6-8. Initiated BIT may be activated by the pilot or a maintenance person. Initiated BIT of systems such as armament and flight controls is not permitted in flight for safety reasons.

Overall status monitoring capability for each avionic system is illustrated in Figure 6-9. Cautions and advisories (e.g., being interrogated on Mode IFF and not replying) as well as BIT information are displayed to the pilot.

The Multipurpose Display provides BIT status information to the pilot from most subsystems as indicated in Figure 6-10; it also serves as a Control Panel for initiated and maintenance BIT and memory inspect.

The Maintenance Monitor Panel, located in the nose wheel well, can handle up to 990 different fault codes and can store up to 62 at any one time. Less than 300 fault codes are currently employed. Pressing the display button commands display of each "tripped" fault code for 1.5 seconds. Releasing the button leaves the code on for 10 seconds, prior to shut off. These fault codes represent the 41 boxes in the

Fighter Aircraft Configuration and 58 in the Attack Configuration plus other related functional failures. Figure 6-11 illustrates selection of maintenance BIT for the SMS.

Initiated BIT tests vary from 50 milliseconds to 150 seconds in the longest case except for special tests such as INS gyro bias setting. Most times are between 2 and 15 seconds.

Memory inspect capabilities which are in the full scale development aircraft and are being considered for production are shown in Figure 6-12. The MC is used to examine the memory of units that are peripheral to the MC and display data for the address selected. This memory inspect capability requires the use of T.O.s and maintenance personnel who are trained in this type of maintenance. If the proper aircraft parameters are recorded during the occurrence of failures, potential benefits to identify intermittents and environmentally induced failures can be achieved. These failures otherwise may have resulted in CNDs and RETOKs. This would permit SRAs with intermittents to be removed from the flight environment until repaired, avoiding future occurrence these problems in "flight-status" aircraft.

Figure 6-13 shows the BIT assurance elements in the F/A-18A design, development, verification and production phases. Production sell-off tests will use the BIT capabilities of the system for maintenance support.

Equipment initial BIT assessment test requirements and results are shown in Figure 6-14. Requirements are shown in the lower left hand corner of the figure. The tests are designed to provide early confidence in the BIT design. Successfully passing the test would provide about a 90 percent confidence level of the design achieving the specified requirements. Percentages are for faults both detected and isolated.

The vendor maintainability/BIT demonstration status on production-configured equipment is shown in Figure 6-15. Figure 6-16 indicates the status of BIT development from flight test program data. Generally, the criterion for "no known BIT design problems" is 30 flights without reoccurrence of the problem.

Figure 6-17 presents the FSD F/A-18A growth trend of unscheduled 0-level maintenance in terms of MMH per FH, currently showing between four and five MMH/FH. Maintenance is performed by contractor personnel; although this will probably degrade in fleet use, the many maintainability features of the F/A-18A show promise of high payoff.

Figure 6-18 displays the FSD F/A-18A mean flight hours between failures showing a progression from 1.3 to 8.4 flight hours. Flights are realistic flights and include typical operational type missions. On the average it takes 4.3 unscheduled 0-level maintenance manhours per flight hour to maintain the aircraft in active flight status.

DISCUSSION POINTS

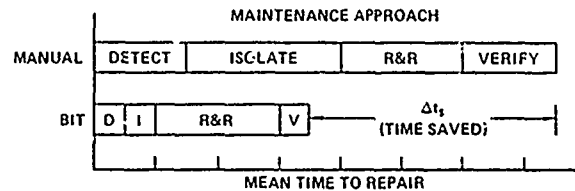
- Failure recordings in the F/A-18A development aircraft include a snapshot of the failed function and aircraft conditions at the time of failure. This proved very useful in BIT development and could be useful in production for troubleshooting intermittent and environmentally induced failures.
- A significant lesson learned from F-15 BIT was to not immediately latch BIT indicators but rather to employ appropriate performance thresholds, time delays, and failure criteria logic prior to declaring "failure".
- The ability to capture intermittents and environmentally induced failures would significantly increase the usefulness of BIT.
- Intermediate-level test compatibility with BIT requires compatibility of thresholds between BIT and I-level testing and the elimination of test voids where possible (including verification of the BIT mechanization).

- At I-level, BIT should be the final test before returning the unit for aircraft service.
- Technology has permitted most avionics subsystems to be mechanized in fewer boxes. Radars, formerly 13-box systems, have been reduced to 4- to 7-box systems. With these boxes becoming more complex, they are more difficult to troubleshoot even though there are fewer of them.
- A concept of Peacetime/Wartime BIT failure criteria levels should be studied for potential future application.
- Reductions in false BIT failure declarations can be achieved by obtaining better quality development data and then properly widening tolerances in thresholds and time delays.
- Some redundancy (but additional unnecessary expense) is incurred by requiring failure indicators on each WRA in aircraft that have a central system failure indication.
- Though the scope that future avionics plays in non-avionic areas such as power control and electro-hydraulic is not specifically defined, it is definitely on the increase and BIT requirements/design need integration in parallel with the system requirements/design.
- The question of determining when a subsystem's BIT is ready to go into development in the aircraft should include a consideration of the percentage design complete and percentage of the software program verified.

F/A-18A AND TF/A-18A AVIONICS BUILT-IN-TEST OBJECTIVES

Figure 6-1

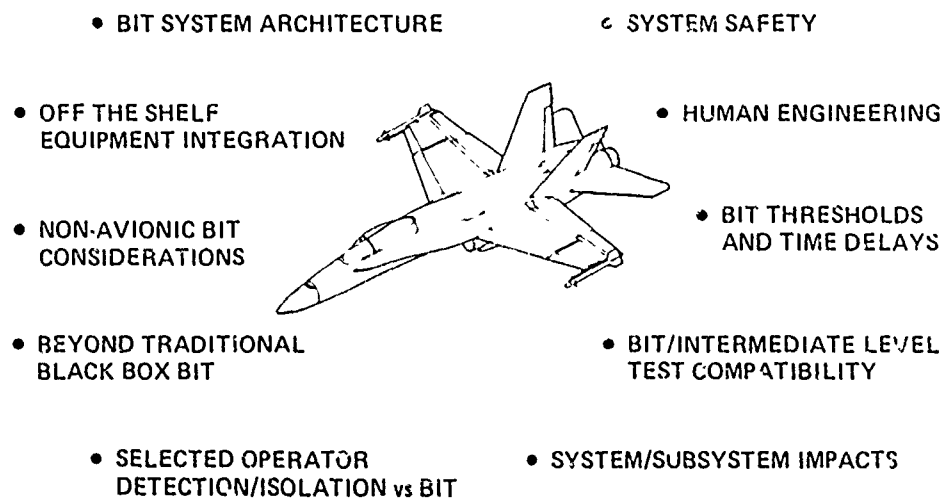
- **INCREASE AIRCRAFT AVAILABILITY**
 - DECREASE DOWNTIME/SHORTEN TURNAROUND TIME
 - AUGMENT SYSTEM MISSION RELIABILITY (HIGHER FLIGHT HOURS/EQUIPMENT OPERATING HOURS)



- **MODERATE SUPPORT (LIFE CYCLE) RESOURCES**
 - MANPOWER
 - TRAINING REQUIREMENTS
 - PERSONNEL SKILLS LEVELS
 - TECHNICAL MANUALS
 - GROUND SUPPORT EQUIPMENT
- **SIMPLIFY AVIONIC SUPPORT ON GROUND AND CARRIER FLIGHT/HANGAR DECKS**
 - ELIMINATE ORGANIZATIONAL GSE
 - REDUCE DECK ACTIVITY
- **ENHANCE AIRBORNE MISSION EFFECTIVENESS**
 - WEAPON SYSTEM CAPABILITY STATUS
 - AUTOMATIC MODE REVERSIONS
 - AIR VEHICLE SAFETY ADVISORIES

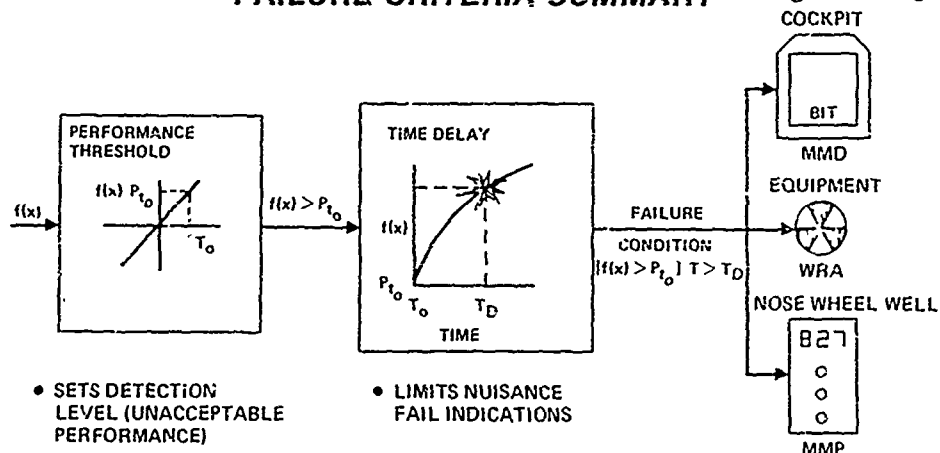
AVIONICS BUILT-IN-TEST INTEGRATION ASPECTS AND DESIGN CONSIDERATIONS

Figure 6-2



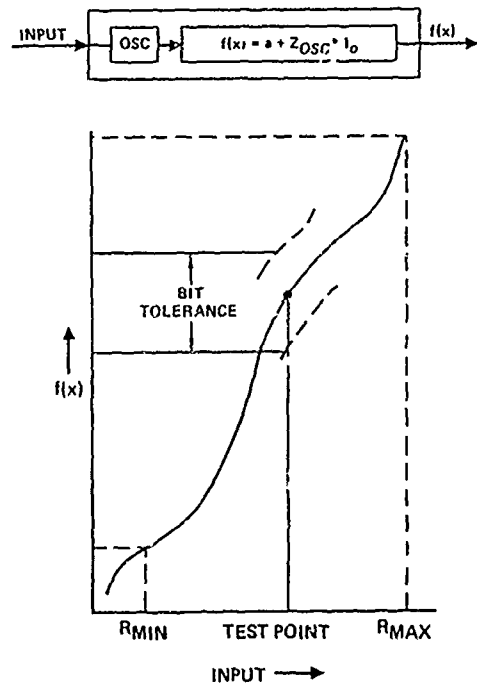
BUILT-IN-TEST FAILURE CRITERIA SUMMARY

Figure 6-3



THRESHOLD DETERMINATION

Figure 6-4



- PROCUREMENT SPECIFICATION

- ENVIRONMENTAL CONDITIONS

- TEMPERATURE
- ALTITUDE
- VIBRATION
- ELECTRICAL

- OPERATING CONDITIONS

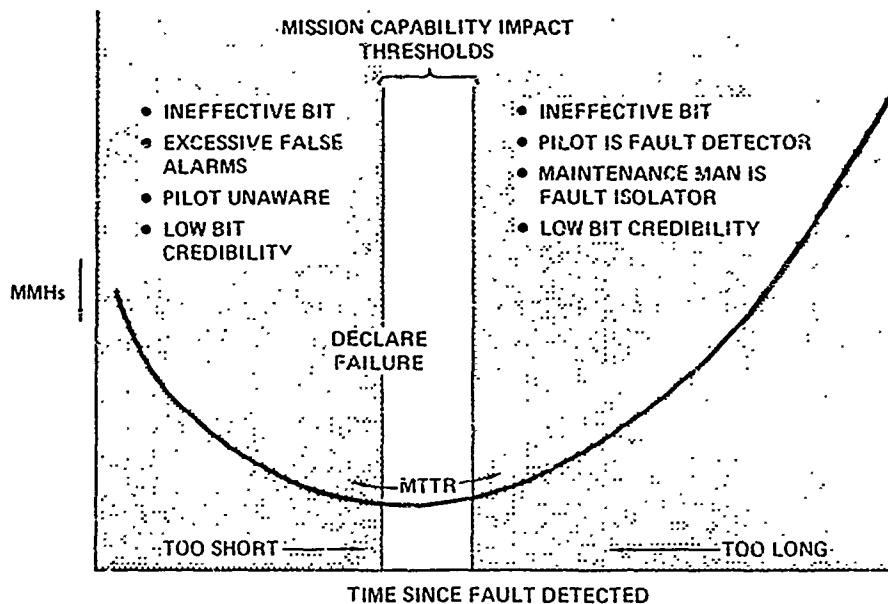
- CARRIER
- LAND BASE
- TAKEOFF
- FLIGHT

Periodic Bit = Normal Operational Check

Initiated Bit = Comprehensive Check (Programmed Tests)

BIT TIME DELAYS

Figure 6-5



F/A-18A AND TF/A-18A AVIONICS BIT SPECIFICATION REQUIREMENTS

Figure 6-6

AIRCRAFT SYSTEM SPECIFICATIONS (SD-565, AR-10)

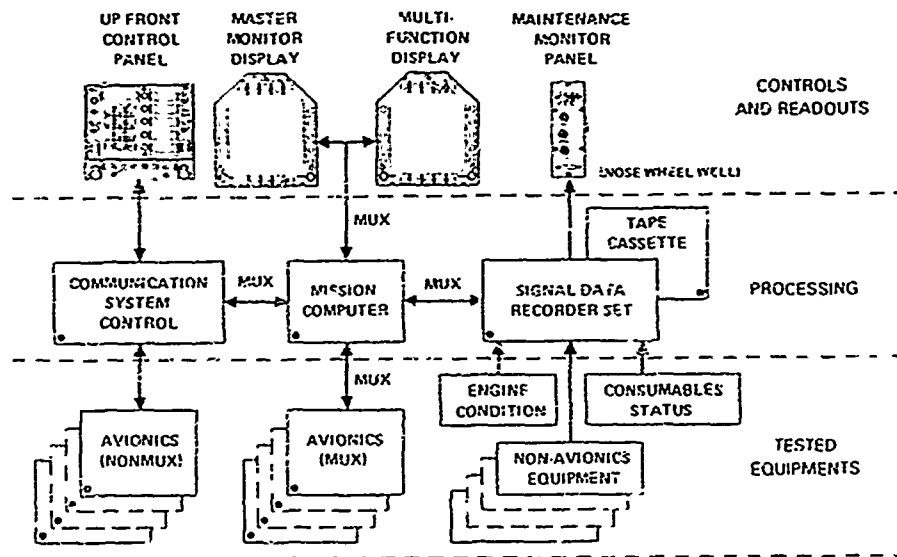
- DETECT/ISOLATE FAILURES (PILOT, WRA, M PANEL)
- ACTIVATE AT EQUIPMENT TURN-ON, MANUAL COCKPIT ACTIVATE
- PREFLIGHT/POSTFLIGHT - NO GSE
- BIT CIRCUIT FAILURES NOT CAUSE OPERATIONAL FAILURES
- INTEGRATE GFE BIT CAPABILITIES
- BIT PERFORMANCE
 - DETECT 98% OF EQUIPMENT FAILURES
 - ISOLATE 95% OF DETECTED TO FAULTY WRA
 - 99% OF FAILURE INDICATIONS CAUSED BY ACTUAL FAILURES

ELECTRONIC EQUIPMENT SPECIFICATIONS (P.S. 74-8700xx)

- IDENTIFY FAILED FUNCTIONS/MODES
- INITIATED BIT COMMANDED BY MC, MAY INTERRUPT OPERATION BUT NOT INTERFERE WITH ASSOCIATED EQUIPMENT
- PERIODIC BIT AT 90% DETECTION
- DISPLAY EQUIPMENT MAY UTILIZE TEST DISPLAYS
- MC WILL ASSIST MULTIPLEX TERMINAL TESTS
- INTEGRATION SIGNALS
 - INPUT ACTIVATE, HOLD, STOP
 - OUTPUT IN TEST, FUNCTION STATUS, WRA FAILED, EQUIPMENT FAILED, EQUIPMENT READY, TEST COMPLETE
- IDENTIFY BIT TEST TIME, CPS, THRESHOLDS, TIME DELAYS
- BIT DESIGN/DEVELOPMENT DATA, ANALYSIS

F/A-18A STATUS MONITORING

Figure 6-7



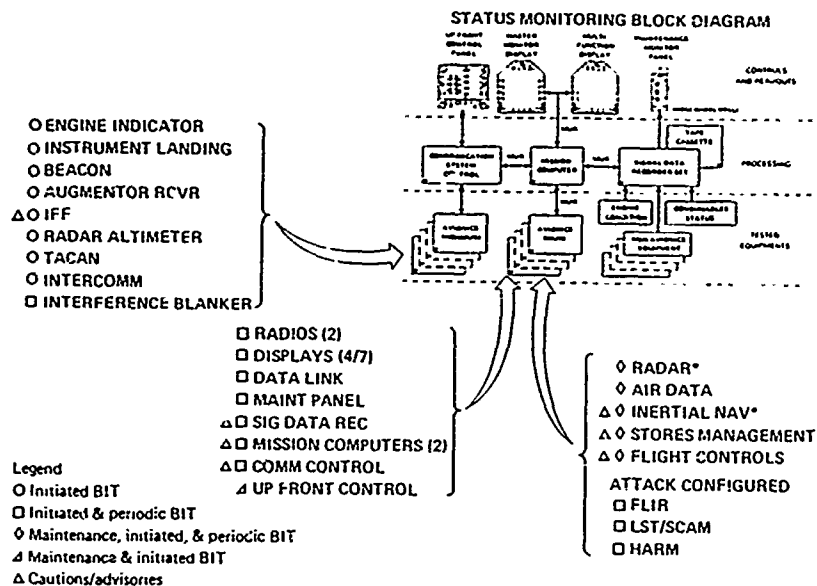
F/A-18A AVIONICS BUILT-IN-TEST OPERATING CHARACTERISTICS

Figure 6-8

- **PERIODIC BIT**
 - AUTOMATIC MONITORING WITHIN SUBSYSTEM AFTER POWER UP
 - HIGH CONFIDENCE OF SUBSYSTEM OPERATING STATUS (90% FAILURE DETECTION)
- **INITIATED BIT**
 - INDIVIDUAL OR SIMULTANEOUS SUBSYSTEM SELECTION BY OPERATOR
 - MAXIMUM FAILURE DETECTION AND ISOLATION CAPABILITY TO REMOVABLE AVIONICS WRA (98% DETECTION)
 - AVAILABLE ON GROUND AND WHERE SAFETY PERMITS IN-FLIGHT
- **MAINTENANCE BIT**
 - CALLS UP SPECIAL CALIBRATION ROUTINES AND DISPLAYS FOR MORE IN DEPTH SUBSYSTEM TESTS
 - EXPANDS FAULT ISOLATION TO PERIPHERAL AIRCRAFT COMPONENTS (RELAY PANELS, FLIGHT CONTROL SWITCHES, ARMAMENT CONTROLS, ETC)
 - AVAILABLE ON GROUND ONLY AND REQUIRES UNIQUE OPERATOR PARTICIPATION

F/A-18A AND TF/A-18A STATUS MONITORING AVIONICS

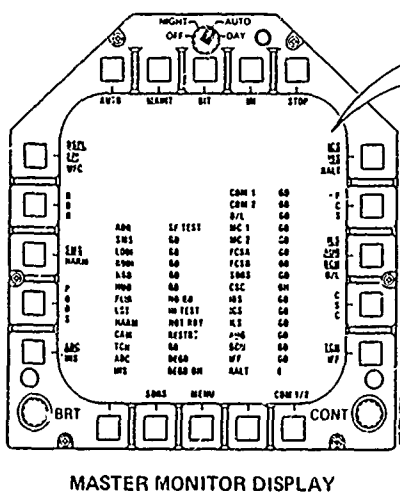
Figure 6-9



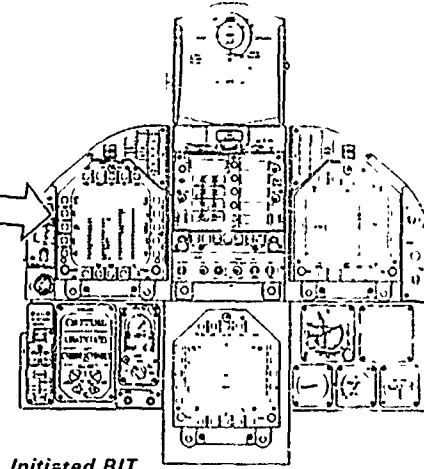
*Maintenance capability in FSD only

AVIONICS BIT DISPLAY Figure 6-10

- Bit tests begin with electrical power "on" and equipment status is reported to rapidly assess mission capability



*Initiated BIT capability not available in-flight



- Status of avionic subsystems available to pilot by selection of BIT display.
- Higher level test may be initiated by pressing button next to subsystem/s legend. All subsystems tested simultaneously by pressing "auto".
- Subsystem status i.e., go, no go, in-test, overheat, degraded, is displayed next to subsystem name.

Figure 6-11

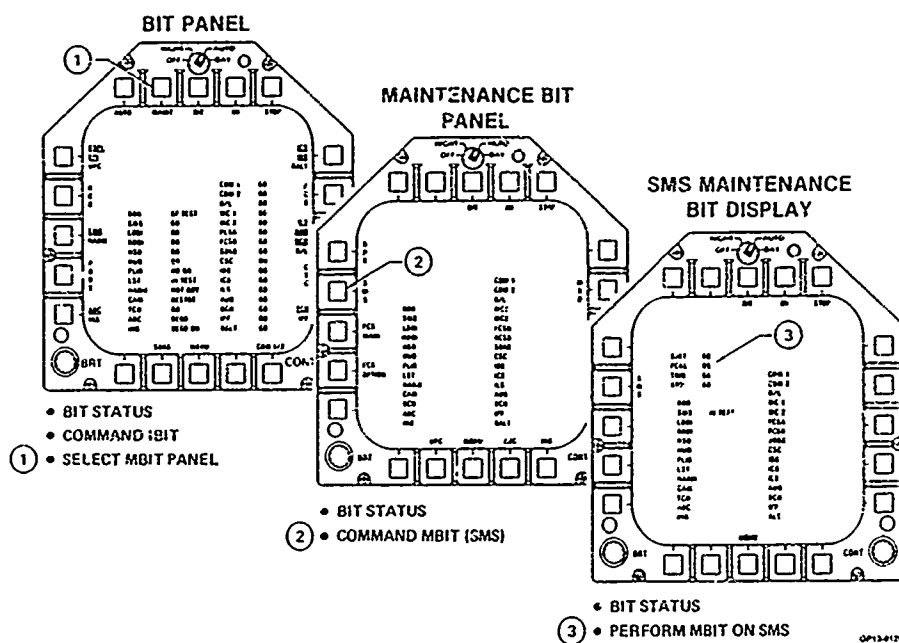
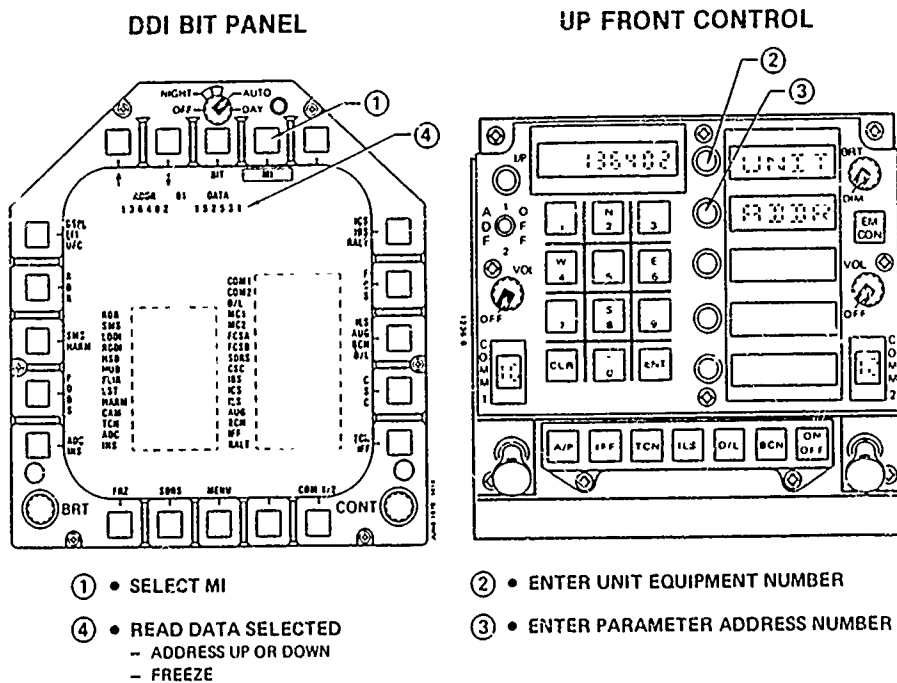


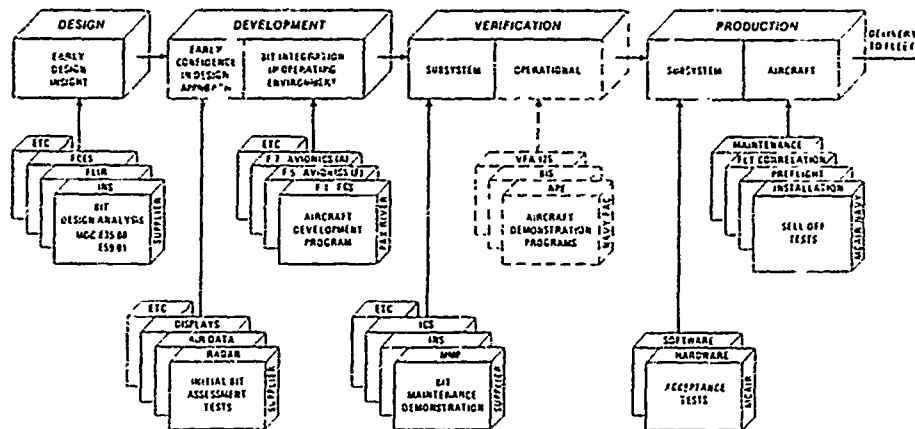
Figure 6-12



*Production incorporation under consideration

F/A-18A AND TF/A-18A BUILT-IN-TEST
ASSURANCE ELEMENTS

Figure 6-13



F-18 AVIONICS

Figure 6-14

EQUIPMENT INITIAL BIT ASSESSMENT REQUIREMENTS/RESULTS

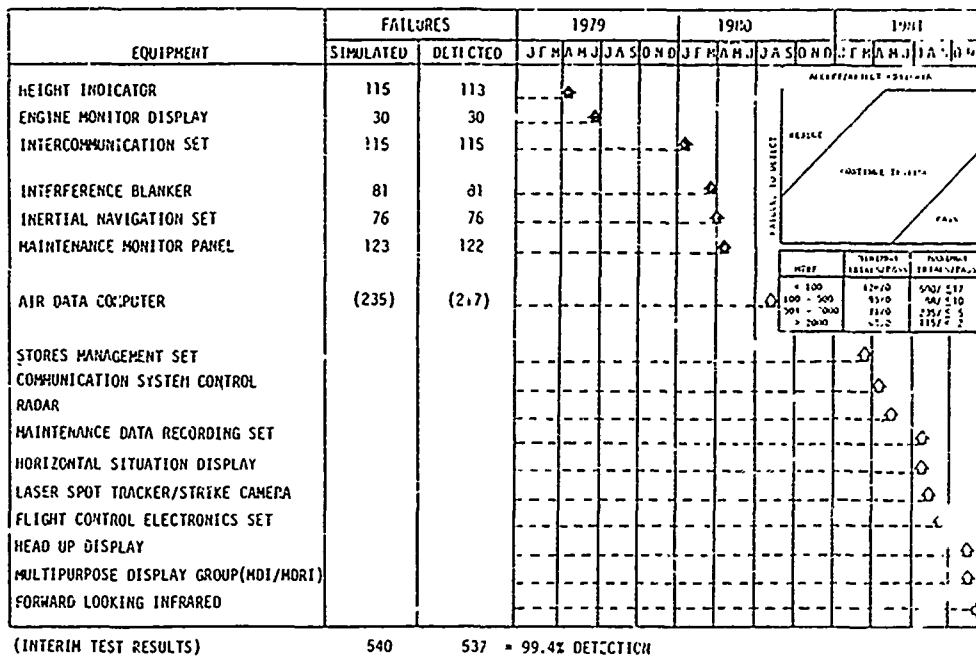
EQUIPMENT	FAILURES			PERCENTAGE DETECTED/ ISOLATED
	SIMULATED DURING TEST	DETECTED/ ISOLATED	NOT DETECTED/ ISOLATED	
MAINTENANCE MONITOR PANEL	58	55	3	95%
INTER-COMM SET	58	47	11	81%
INERTIAL NAVIGATION SET	131	126	5	96%
ENGINE MONITOR DISPLAY	112	112	0	100%
HEAD-UP DISPLAY	118	110	8	93%
AIR DATA COMPUTER	118	117	1	99%
INTERFERENCE BLANKER	125	125	0	100%
COMMUNICATION SYSTEM CONTROL	118	118	0	100%
MULTI-PURPOSE DISPLAY GROUP	118	118	0	100%
MAINTENANCE SIGNAL DATA RECORDER	118	116	2	98%
STORES MANAGEMENT SET	118	109	9	92%
FLIGHT CONTROL ELECTRONICS	118	105	13	89%
RADAR	302	243	59	80%
SUMMARY:				
o TOTALS	1612	1501	111	93%
o BIT FIXES REQUIRED			9	
o DETECTION PERCENTAGE WITH FIXES				99%

REQUIREMENTS	
EQUIPMENT MTBF	NO. OF SIMULATED FAILURES/UNDETECTED
<100	300/3
100 to 500	194/2
501 to 2000	118/1
>2000	58/1

Figure 6-15

F/A/TF-18 MAINTAINABILITY/BIT DEMONSTRATION STATUS

31 JANUARY 1981



F-18 BUILT-IN-TEST AIRCRAFT INTEGRATION AND DEVELOPMENT

6 FEBRUARY 1981

Figure 6-16

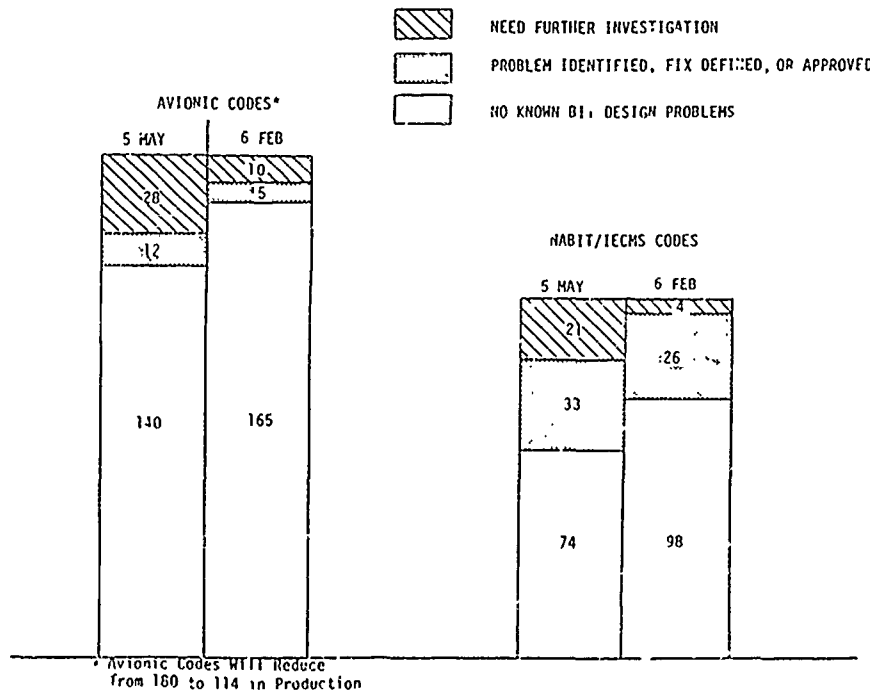
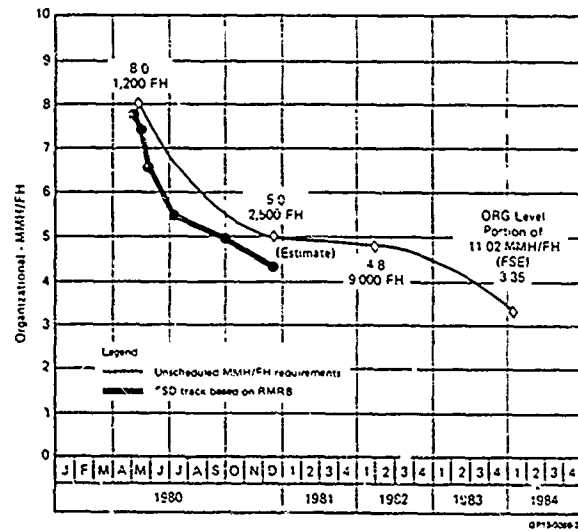
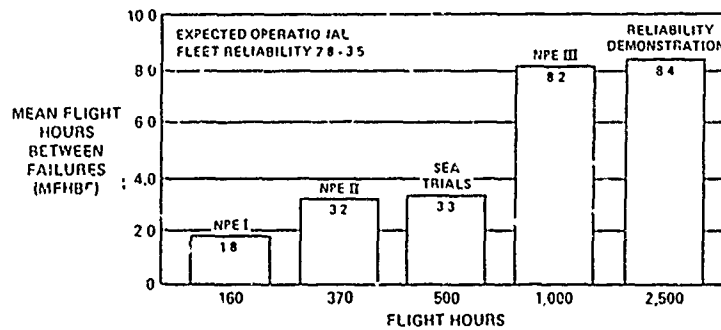


Figure 6-17



CF-18 HORNET

**F/A-18A RELIABILITY SUMMARY
THROUGH 3,000 HOURS OF TEST EVALUATION Figure 6-18**



- 1979 FLEET EXPERIENCE F-4J = 0.69 MFHBF, A-7E = 0.95 MFHBF
- CUMULATIVE TEST EXPERIENCE - OPERATIONAL TYPE GROUND RULES = 2.5 HR MFHBF (ALREADY BETTER THAN A-7 AND F-4J)
- F/A-18A ACHIEVED ITS RELIABILITY REQUIREMENTS BY COMPLETING THE 50 FLIGHT (100 FLIGHT HOURS) RELIABILITY DEMONSTRATION WITH AN 8.4 HR MFHBF (3.7 REQUIRED)

GP130100-36

AN/AYK-14(V) BUILT IN TEST

Wei Long Chen
CONTROL DATA CORPORATION

Mr. Chen is a Senior
Diagnostics Engineer with
Control Data Corporation

HIGHLIGHTS OF THE PRESENTATION

The BIT development sequence for the AN/AYK-14(V) is shown in Figure 7-1. AN/AYK-14 BIT is implemented in firmware, as shown in Figure 7-2, using the CDC 480 minoprocessor. BIT performance capabilities are shown in Figure 7-3, including the fault isolation within the 5.0 milliseconds. The BIT indicator stays if power is removed before indication is recorded. Fault isolation requirements in the Navy specification are 86 percent to one card and 93 percent to two cards. No fault detection requirements were specified. The MTTR and MTBF requirements specified were not included in the BIT requirements.

Central Processing Unit, Input Output Processors, and Extended Arithmetic Unit performance capabilities are shown in Figures 7-4, 7-5, and 7-6.

Design verification was accomplished by a preliminary qualification test including algorithm evaluation, code review, a function test and a system test and by a formal qualification test incorporating customer concurrence that all requirement specifications have been met. The BIT Design Review Board consisted of representatives from Government and from the areas of firmware, diagnostic, and hardware design as well as quality assurance and reliability and maintainability. Algorithm evaluation was accomplished by review of design flow charts, verification that the program design addressed the fault detection and isolation specification, and finally the generation of a report. Code review was accomplished by verification

that the code is error-free, that it complies with the standards and conventions, that it implements the approved design specs, and finally the generation of a report. Microcode programs were checked by other microcode programmers. The BIT code is contained within a 512 32-bit micro-memory.

Function tests were performed as shown in Figure 7-7. Faults were selected by CDC. Software diagnostics were used as a backup to firmware BIT for the system test fault list. System test was performed as shown in Figure 7-8. Formal qualification tests were performed as shown in Figure 7-9. The government selected 331 faults and witnessed these tests. BIT firmware has been accepted by the government.

AN/AYK-14(V) BUILT-IN-TEST DEVELOPMENT SEQUENCE

- NAVY REQUIREMENTS
- CONTROL DATA PROPOSAL
- CONTRACT
- PROGRAM PERFORMANCE SPECIFICATION
- INTERFACE DESIGN SPECIFICATION
- PROGRAM DESIGN SPECIFICATION
- ALGORITHM EVALUATION
- IMPLEMENTATION
- CODE REVIEW
- FUNCTION TEST
- SYSTEM INTEGRATION TEST
- RELEASE TO CONFIGURATION MANAGEMENT
CONTROL
- FORMAL QUALIFICATIONS TEST
- BASELINE

Figure 7-1

AN/AYK-14(V) COMPUTER SYSTEM BUILT-IN-TEST

- BUILT-IN-TEST IS PART OF AN/AYK-14(V) FIRMWARE
- BUILT-IN-TEST FIRMWARE RESIDES IN
MICROMEMORY
- COMPUTER ELEMENTS WITH BUILT-IN-TEST
 - CENTRAL PROCESSING UNIT (CPU)
 - INPUT/OUTPUT PROCESSOR (IOP)
 - EXTENDED ARITHMETIC UNIT (EAU)

Figure 7-2

BIT PERFORMANCE SPECIFICATIONS

OVERALL PERFORMANCE

- INITIATED ON POWER-UP, MASTER CLEAR, INITIAL PROGRAM LOAD (IPL)
- EXECUTES IN LESS THAN 5.0 MILLISECONDS
- SETS BIT INDICATOR WHEN ERROR ENCOUNTERED
- PROVIDES STATUS/ISOLATION CODE WHEN ERROR IDENTIFIED

Figure 7-3

CPU BIT PERFORMANCE SPECIFICATION

- INITIATED AS A RESULT OF
 - SYSTEM POWER-UP
 - HARDWARE MASTER CLEAR
 - CONTROL CONSOLE MASTER CLEAR
 - INITIAL PROGRAM LOAD (IPL)
- TEST SCOPE
 - MICROSEQUENCE
 - ARITHMETIC LOGICAL UNIT (ALU) REGISTERS, U, K, AND I REGISTERS
 - ALU LOGIC NETWORK
 - FILE AND C-FILE
 - MEMORY CONTROL MODULE (MCM) PAGE FILE
 - CPU BUS AND I/O BUS
 - EVENT MONITOR
 - MEMORY PARITY
- SETS BIT INDICATOR WHEN ERROR DETECTED, AND
 - IF COMPUTER SUPPORT EQUIPMENT (CSE) IS CONNECTED, FIRMWARE HANGS AND AN ERROR IDENTIFICATION CODE IS SENT TO CSE FOR DISPLAY.
 - IF NO CSE IS CONNECTED, BIT RESTARTS.
- STARTS THE SYSTEM INITIALIZATION PROCESS IF BIT SUCCESSFULLY COMPLETES.
- IN A DUAL PROCESSOR CONFIGURATION, CHECKS IF IOP BIT RAN TO SUCCESSFUL COMPLETION. FIRMWARE HANGS, IF IOP FAILS ITS BIT.

Figure 7-4

IOP BIT PERFORMANCE SPECIFICATION

- INITIATED AS A RESULT OF
 - SYSTEM POWER-UP
 - MASTER CLEAR
- TEST SCOPE
 - MICROSEQUENCE
 - ALU REGISTERS, U, K, AND I REGISTERS
 - ALU LOGIC
 - FILE
 - I/O BUS
 - EVENT MONITOR
 - MEMORY INTERFACE
- SETS BIT INDICATOR WHEN ERROR DETECTED, AND
 - IF CSE IS CONNECTED, FIRMWARE HANGS AND AN ERROR IDENTIFICATION CODE IS SENT TO CSE FOR DISPLAY.
 - IF NO CSE IS CONNECTED, BIT RESTARTS.
- INFORMS CPU OF IOP TEST STATUS IN A DUAL PROCESSOR CONFIGURATION.
- STARTS IOP INITIALIZATION PROCESS IF BIT IS SUCCESSFULLY COMPLETED.

Figure 7-5

EAU BIT PERFORMANCE SPECIFICATION

- INITIATED BY CPU BIT
- TEST SCOPE
 - ARITHMETIC LOGICAL UNIT (ALU)
 - PROGRAMMABLE READ ONLY MEMORY (PROM) CONSTANTS CHECKSUM
 - EXPONENT ALU LOGIC
 - CONDITIONAL REGISTER AND BRANCH LOGIC
 - REGISTER SHIFT LOGIC
 - REGISTER MULTIPLY LOGIC
- SETS ERROR FLAG IN STATUS WORD, AND AN ERROR IDENTIFICATION CODE IS SENT TO CPU.
- ON EXIT (NORMAL OR ABNORMAL) FIRMWARE ENTERS IDLE LOOP TO WAIT FURTHER PROCESSING.

Figure 7-6

FUNCTION TEST

• TEST REQUIREMENTS

- COMPUTER SUPPORT EQUIPMENT IS REQUIRED TO CONTROL BIT EXECUTION.
- RELIABILITY AND MAINTENANCE GROUP PROVIDES A LIST OF FAULTS THAT INCLUDES AT LEAST ONE FAULT TO EXERCISE EACH ERROR STOP IN BIT FIRMWARE.

Figure 7-7

• TEST PROCESS

- HARDWARE DESIGN GROUP APPROVES THE FAULTS.
- FAULTS ARE INSERTED ON IC CHIP LEADS.
- VERIFIES THAT THE DETECTED FAULTS ARE ISOLATED CORRECTLY.
- EACH UNDETECTED FAULT IS ANALYZED TO DETERMINE ITS RELEVANCE TO FUNCTIONAL PERFORMANCE.
- CORRECTS BIT FIRMWARE TO PROVIDE DETECTION OF THE RELEVANT FAULTS.
- GENERATES REPORT.

- THE UNDETECTED FAULTS RELEVANT TO FUNCTIONAL PERFORMANCE ARE ADDED TO THE SYSTEM TEST FAULT LIST.

SYSTEM TEST

• TEST REQUIREMENTS

- COMPUTER SUPPORT EQUIPMENT IS REQUIRED TO CONTROL BIT AND DIAGNOSTICS SOFTWARE EXECUTION.
- RELIABILITY AND MAINTENANCE GROUP PROVIDES A LIST OF FAULTS.

• TEST PROCESS

- FAULTS ARE INSERTED INTO IC CHIP LEADS.
- BIT SUPPLEMENTED BY THE DIAGNOSTICS SOFTWARE IS RUN.
- EACH UNDETECTED FAULT IS ANALYZED TO DETERMINE ITS RELEVANCE TO THE SYSTEM PERFORMANCE.
- CORRECTS DIAGNOSTICS PROGRAMS, BIT OR DIAGNOSTICS SOFTWARE, TO PROVIDE THE DETECTION OF THE RELEVANT FAULT.
- GENERATES REPORT.

Figure 7-8

FORMAL QUALIFICATION TEST

- TEST REQUIREMENTS

- COMPUTER SUPPORT EQUIPMENT IS REQUIRED TO CONTROL BIT AND DIAGNOSTICS SOFTWARE EXECUTION.
- THREE DIFFERENT AN/AYK-14(V) CONFIGURATIONS ARE REQUIRED TO UNDERGO THIS TEST.
- GOVERNMENT PROVIDES A LIST OF FAULTS.
- THIS TEST MUST BE WITNESSED BY GOVERNMENT REPRESENTATIVES.

Figure 7-9

- TEST PROCESS

- FAULTS ARE INSERTED.
- ON EACH CONFIGURATION, BIT SUPPLEMENTED BY ITS DIAGNOSTICS SOFTWARE IS RUN.
- ALL FAULTS THAT ARE NOT DETECTED OR ISOLATED CORRECTLY ARE ANALYZED FOR THEIR LEGITIMACY.
- GENERATES REPORT.

AN/ALG-126B
DESIGNING AND VALIDATING BIT

Ken Wilson
MAINTENANCE TECHNOLOGY, INC.

Mr. Wilson is President
of Maintenance Technology,
Inc.

HIGHLIGHTS OF THE PRESENTATION

The requirements evolution of the AN/ALG-126B has derived from recent experience with the AN/ALQ-126 and the AN/ALR-45, and fleet availability experience. RISE (Readiness Improvement Scales Evaluation) of the ALQ-126 and the ALR-45 provided high level visibility indicating the requirement for improvements. Both were specified by AR-10 criteria to 99 percent fault detection and 98 percent fault isolation. With ECM equipment, the only performance verification is provided by BIT or by ETE, which makes BIT very important. A 34 percent CND rate or removed SRAs at "I" level was observed in operation of the ALQ-126. In 1978, all boxes were removed from the aircraft and put through a mod program; BIT was the first test performed on the removed units. In the ALQ-126 mod program (Delta-Mod), 46 percent of the units removed had "hard" failures by I-level tests, although the BIT had showed them to be good. In the Colt-45 mod program--the ALR-45 update--55 percent of the boxes actually had hard failures that the BIT showed to be good. In both cases, validity of the hard failures was established by the I-level tests.

It appears that false alarm problems early in the programs may have resulted in the spread of tolerances in the BIT, reducing its effectiveness. In certain RF areas where BIT was not effective, reliance was placed on external test equipment.

For the ALQ-126, I-level bench testing initially resulted in an overall field MTTR of approximately 10 hours. That was

subsequently reduced to 8 hours, but never achieved the laboratory demonstrated MTTR of 2 hours.

The parameters specified for the AN/ALQ-126B are shown in Figure 8-1. MTTR was specified as 30 minutes at O-level and 2 hours at I-level. The same AR-10 values were imposed as with the ALQ-126. I-level testing was required to use the same logic and circuitry as the BIT.

To ensure timely validation of the ALQ-126B BIT, a design review team was established. This team was made up of an experienced systems engineer, dedicated subsystems engineers, a test equipment engineer and a field engineer. In-process validation of the AN/ALQ-126B is shown in Figure 8-2.

The joint verification process of the AN/ALQ-126B is shown in Figure 8-3, using each requirement of the specification. No specific cutoff point (e.g., 10 percent) for BIT was established. The maintainability demonstration has not been completed since the equipment is presently in T&E.

Figure 8-4 provides an example of ALQ-126B BIT paper verification as related to the specification requirements.

BIT effectively is presented in Figure 8-5, showing an overall BIT effectivity of 96.5 percent. Comparisons between the ALQ-126 and the ALQ-126B are shown in Figure 8-6. The most significant improvements are shown in the increased number of fault indications (38 to 170), the decreased percent of dedicated BIT hardware (20 percent to 2 percent), and the increased percent of BIT circuitry tested by BIT (1 to 99 percent). It should be noted that the ALQ-126 is basically an analog box and the ALQ-126B is primarily a digital box. Utilization of BIT logic at I-level was increased from 0 to 95 percent. Interface circuitry, which provides for future wraparound BIT, has been included to accommodate inputs from other interfacing units.

DISCUSSION POINTS

- Functions tested are identified by specific circuit analysis.
- BIT effectivity is expressed numerically.
- O-level test equipment dependence has been reduced.
- I-level test time has been reduced, using the same logic from O-level to I-level.
- False removal rate is projected to be less than one percent.
- Cost for the dedicated BIT engineering is approximately five percent of the non-recurring costs. An anticipated reduction in production testing costs will more than offset the development investment. In addition, the O-level and I-level non-recurring and recurring test equipment costs have been reduced by use of BIT.
- There is initial design opposition to BIT that may be overcome by successful use of BIT in the debug process.
- Management (government and contractor) must be educated early in the program and informed of the significant cost benefits achievable by incorporation of BIT early in the design phase.
- Defining a BIT FOM should include the number of functions tested, the amount of BIT required to test the functions, the reliability of the BIT circuitry and the accuracy of the BIT measurement.
- If a parameter is sufficiently important to be specified for BIT monitoring, the tolerances for BIT monitoring should also be specified.
- Partitioning of equipment by function must be considered in terms of BIT operation.

AN / ALQ-126B REQUIREMENTS EVOLUTION

● SPECIFIED PARAMETERS

- BIT ACCURACY (WITHIN 10% OF SPEC VALUES)
- MTTR
- AR-10 (% FAULT DETECTION/ISOLATION)

● GOALS

- "0" LEVEL TEST EQUIPMENT
 - ELIMINATE
- "I" LEVEL TEST PHILOSOPHY
 - MINIMIZE BENCH LOADING

Figure 8-1

AN / ALQ-126B IN-PROCESS VALIDATION

● CONTRACTOR — PROGRAM MANAGEMENT IMPLEMENTATION

- PERSONNEL SELECTION
 - SYSTEM ENGINEER
 - SUB-SYSTEM ENGINEERS
 - HARDWARE
 - SOFTWARE
 - TEST EQUIPMENT
 - TRAINING
- DESIGN REVIEW PROCESS
- RESOURCE ALLOCATIONS

Figure 8--2

**AN / ALQ-126B
JOINT VERIFICATION**

- SPECIFICATION ITEM REVIEW
- BIT CONTRIBUTION TO FAILURE RATE
- BIT EFFECTIVITY
- "O" LEVEL TEST EQUIPMENT REQUIREMENTS
- "I" LEVEL BENCH TIMES
- MAINTAINABILITY DEMONSTRATION

Figure 8-3

EXAMPLE OF ALQ-126 BIT "PAPER" VERIFICATION

SPECIFICATION PARA	SPECIFICATION REQUIREMENT DESCRIPTION	NOT APPLICABLE	NOT CHECKED	SELF TEST CHECKS																
				01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
35.1.1.1.2.1.1	RF Characteristics RF Stable RF Unstable RF Agile	•					•	•	•	•	•	•	•	•	•	•	•	•	•	•
35.1.1.1.2.1.2	PRF Characteristics PRF Stable PRF Unstable Random PRF Agile Patterned PRF Agile PRF Staggered		•									•								
35.1.1.1.2.2	Emitter Parameter Limits																			
35.1.1.1.3	Multiple Signal Handling																			
35.1.1.1.3.1	Signal Tracking Capability																			
35.1.1.1.3.1.1	Precision Agile TOA Tracking																			
35.1.1.1.3.1.2	Coarse TOA Tracking	•																		
35.1.1.1.3.1.3	Stable RF Tracking																			
35.1.1.1.3.1.4	Stepped RF Agile Tracking																			
35.1.1.1.4	System Response Time		•																	
35.1.1.2	ECM Receiver Requirements	•																		
35.1.1.2.1	RF Threshold and Sensitivity																			
35.1.1.2.1.1	Scan Modulation Recovery																			
35.1.1.2.1.2	Receiver Protection		•																	
35.1.1.2.2	RF Processing Requirements	•																		
35.1.1.2.2.1	Repeater Processing Requirements	•																		
35.1.1.2.2.1.1	Memory Repeater																			
35.1.1.2.2.2	Transponder Processing Requirements	•																		
35.1.1.2.2.2.1	RANRAP																			
35.1.1.2.2.3	Combination Processing Requirements	•																		
35.1.1.2.2.4	BIT Requirements	•																		
35.1.1.2.3	Output Characteristics	•																		
35.1.1.2.3.1	RF Dynamic Range and Output Power																			
35.1.1.2.3.2	Pulse Width																			
35.1.1.2.3.3	Duty Factor																			
35.1.1.2.3.4	Repeater Response Time																			
35.1.1.3	System Resources																			
35.1.1.3.1	Frequency Bands	•																		

Figure 8-4

AN / ALQ-126B BIT EFFECTIVITY DERIVATION

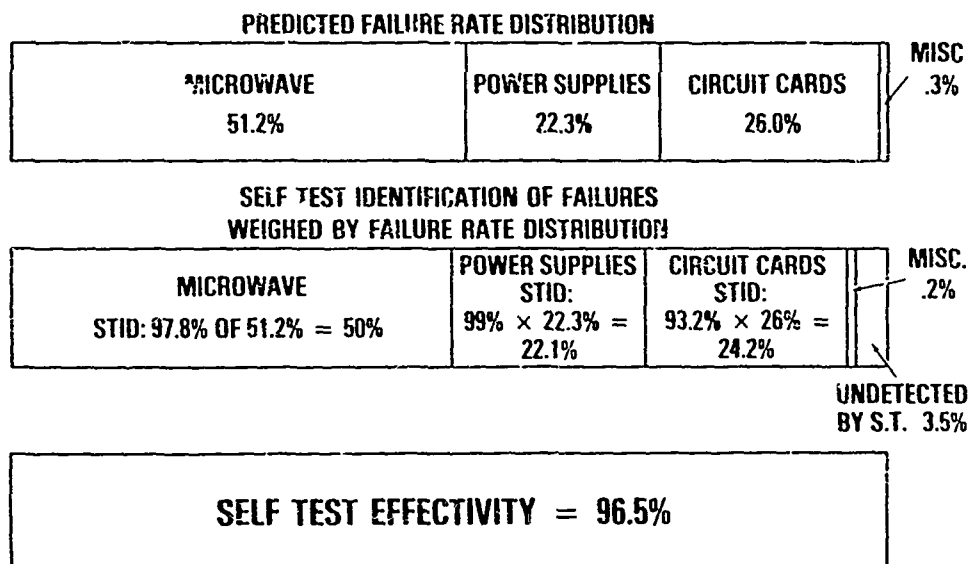


Figure 8-5

AN / ALQ-126B VERIFICATION

<u>COMPARISON TO AN / ALQ-126</u>	<u>126</u>	<u>126B</u>
NUMBER FUNCTIONAL TESTS (FAULT DETECTION)	3	7
MAJOR TEST CASES (RF POWER, SENSITIVITY, ETC)	5	11
SPECIFIC TESTS (RF POWER SATURATION AND MIN SIGNAL)	31	53
NUMBER FAULT INDICATIONS (RF FIRST, SECOND AMP, OUTPUT AMP)	38	170
% BIT DEDICATED HARDWARE	20%	2%
% BIT TESTED BY BIT	<1%	99%
ANALYTICAL DIAGNOSTICS ("I" LEVEL UTILIZATION OF BIT LOGIC)	0	95%
BIT PROVISIONS FOR INTERFACE CIRCUITRY	0	80%

125/126 Figure 8-6

AN/SPS-67 RADAR BIT

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John Rogers, NAC

Mr. Nunn is the head of the Test Technology Office at NOSC. Mr. Rogers is a test equipment engineer at NAC.

HIGHLIGHTS OF THE PRESENTATION

The AN/SPS-67 radar is a Class A surface search radar which replaces the AN/SPS-10. It was developed by NORDEN, a division of United Technologies, under NAVSEA contract. The radar completed operational evaluation in October-November 1980. It originated from an exploratory development program that showed that life cycle costs (LCC) of Navy radar systems could be reduced by 50 percent, using the technology of 1972. This program was called "2175," "two to one in 1975." The AN/SPS-67 radar was one of the four projects in the 2175 program. At the time of exploratory development there were fifty-plus radars all performing the same surface search function. Analyses showed that the functions of all these radars could be performed by two radars which would be ninety-five percent alike. The radars were partitioned functionally, using 46 types of Navy standard electronic modules (SEMs) many of which had already been developed by NAC; approximately 29 SEMs had to be developed specifically for this program. BIT and design for testability had been specified as a requirement during the 6.1 and 6.2 phases, and implemented in the 6.3 phase. In the fleet today there are 4 to 5 million SEMs in over 150 types of equipment. Testability (as in reliability, maintainability, and availability) requires a firm technology base to support the systems in which it is incorporated.

NAC developed the exploratory development model which was delivered and qualified prior to going out on contract to

Norden. It consisted of six units, including the dummy load and remote control unit. The major units were the video processor and the receiver transmitter.

BIT requirements for the AN/SPS-67, as specified in SHIPS-R-5763A, are that it shall locate 95 percent of failures to the four SEMs in either the video processor or the receiver-transmitter; that it shall have at least two operating modes (normal, operational and interactive, test); and that it have automatic self-test. Other specified BIT requirements are shown in Figure 9-1. Automatic self-test includes testing of 274 test points every 20 seconds. Double fault testing also is used. After double verification of the fault, the BIT further checks the fault an additional 16 times. If it still exists at that time, a hard fault is declared and an alert is displayed to the operator and the fault identification information is recorded on the maintenance panel. Figure 9-2 identifies the requirements specified for the interactive BIT. The operator can select a test point at random and step through test points one-at-a-time around the selected point. Figure 9-3 indicates the specified testability requirements of which BIT is a subset. Figure 9-4 indicates the specified maintainability requirements.

Maintainability program characteristics are shown in Figure 9-5. NAVSEA Detachment, Norfolk, appointed one person to follow the program throughout with regard to its maintainability, thereby providing continuity to the program. Characteristics specified for maintenance personnel are that they hold an ET3 maintenance rating, be a graduate of an applicable Class "C" school, and have nine months related experience. A Navy ET3 is equivalent to an Air Force E4. "C" school runs from two to six weeks on a particular piece of gear (the SPS-67 required two weeks). The specification of qualifications of the maintenance personnel results primarily in the level

of writing of the maintenance manuals. It does not appear to drive the equipment design over and above the specified MTTR.

Results of BIT showing isolation to an average of four SEM ambiguity level is shown in Figure 9-6, with BIT comprising 20 percent of the total circuitry. A more intensive BIT is being developed for the digital section, whereby a known signature is introduced into the front end and later read out after processing and compared with the known desired signatures.

Verification of BIT was performed through a factory maintainability demonstration conducted by a Navy ET3 personnel using actual clock time. A total of 57 tasks were selected. Factory tests showed an MTTR of 30.3 minutes. Maintainability tests resulted in an MTTR of 22 minutes. The evaluation of radar reliability estimated a 3,000 hour MTBF. In actual tests, the radar demonstrated 2,895 hours with one failure.

DISCUSSION POINTS

- The Advanced Technology Strategy Team is a Navy strategy team consisting of representatives from every Navy laboratory and most of the field activities, resulting in a total of 20-plus organizations. The team meets on a quarterly basis, planning and implementing the basic research programs in the Navy. Test technology is being considered in the 6.1, 6.2, and 6.3 funding categories, especially those things which are considered critical to the Navy. One of the documents that the team has generated is the "BIT Design Guide." It includes a "strawman" spec for specifying BIT, and BIT-related definitions. A false alarm is considered a failure as defined in this guide. The guide is available, on request, through NOSC.
- Testability and BIT requirements should prevail throughout the specification of a system, using previous experience with similar systems to determine where BIT requirements should be made more specific (e.g., VSWR on a duplexer). Design reviews should be used to refine decisions on implementation of BIT.

- NWSOC has developed a two day training course termed "Design for Testability" which has recently been presented at the Navy Postgraduate School. The course will be offered around the country to government and industry. It includes testability needs and details on techniques to make designs testable. It also includes analog, digital and hybrid circuits. It deals with both system level and board level testability. Measurements of achieved testability capabilities are also included. The schedule for offering the course has not been established. (Notification will be sent to all BIT workshop attendees. Other details on the course are available from Bill Keiner at the NWSOC.)
- A Test Technology Library has been established at NOSC including information on such areas as electro-optics, fiber optics, bubble memories, microprocessor-based boards, etc. The data base for the design for testability has been provided to the library through Bill Keiner at the NWSOC.
- A "corporate memory" has been established by the Navy, having a focal point of one or more individuals at each laboratory and fleet center (e.g., NEC, Charleston Engineering Center, and the Fleet Training Equipment Center, Orlando). Quarterly meetings are held among members with assignments for program reviews, etc. For basic research (6.1), contact is maintained with various university professors as part of the "corporate memory", encouraging them to incorporate design for testability into the curriculum to address long-term problems. However, short-term and medium-term problems cannot be handled by this approach.

SPECIFIED BIT

Figure 9-1

- o FAILURE SHALL NOT DEGRADE SYSTEM PERFORMANCE
- o SHALL DISPLAY LOCATIONS OF FAULT ON INDICATORS
- o SHALL ALERT OPERATOR OF MARGINAL OPERATION
- o SHALL BE CAPABLE OF MEASURING AND DISPLAYING SPECIFIED FUNCTIONS

SPECIFIED INTERACTIVE TEST BIT

Figure 9-2

- o SHALL NOT REQUIRE EXTENSIVE OPERATOR INTERFACE
- o SHALL ALLOW FOR SELECTION OF SENSOR TEST POINTS
- o SHALL ALLOW SEQUENTIAL STEPPING OF TEST EVENTS

SPECIFIED TESTABILITY CHARACTERISTICS Figure 9-3

- o MODULATOR - TRANSMITTER SHALL HAVE FAULT DETECTION SENSORS FOR BIT MONITORING
- o DIRECTIONAL COUPLER SHALL CONTAIN PROVISIONS FOR BIT AND EXTERNAL TEST EQUIPMENT
- o VIDEO OUTPUTS FROM VIDEO DISTRIBUTION AMPLIFIERS SHALL BE AVAILABLE FOR BIT

SPECIFIED MAINTAINABILITY CHARACTERISTICS

Figure 9-4

- o MTTR SHALL NOT EXCEED .5 HOUR
- o MAX TTR SHALL NOT EXCEED 1.5 HOURS AT THE 95TH PERCENTILE

SPECIFIED MAINTAINABILITY CHARACTERISTICS

Figure 9-5

- o MAINTAINABILITY PROGRAM PER MIL-STD-470
- o MAINTAINABILITY PREDICTION PER MIL-HDBK-472
- o MAINTAINABILITY DESIGN REVIEW
- o DESIGN AND CONSTRUCTION SHALL PERMIT RAPID ASSEMBLY AND DISASSEMBLY FOR EASE OF MAINTENANCE

RESULTS

Figure 9-6

- o AVERAGE AMBIGUITY OF FOUR SEM
 - ONE ANALOG
 - FIVE TO SEVEN DIGITAL
- o APPROXIMATELY 20% OF TOTAL CIRCUITRY IS BIT
- o NO "O" LEVEL TEST EQUIPMENT REQUIRED
- o NO FALSE ALARMS DURING OP/TECH EVALUATION
- o 274 TEST POINTS
- o SIGNATURE ANALYSIS CURRENTLY BEING DEVELOPED
FOR DIGITAL SECTION

THE U.S. NAVY'S AEGIS
WEAPONS SYSTEM-ORTS

Howard Boardman
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HIGHLIGHTS OF THE PRESENTATION

The AEGIS weapon system (Mark 7) consists of a weapons control system, command and decision center, a radar system (AN/SPY-1A), an operational readiness test system, standard missile, guided missile launching system, and a fire control system. The key performance factors of the AEGIS are reaction time, firepower, ECM and environmental resistance, coverage, and continuous availability.

Real world availability is described in Figure 10-1. Requirements were allocated to various portions of the system. The system design process is shown in Figure 10-2 showing the relationship between the FMEA and the availability model analysis. The test design requirements are allocated to ORTS and BIT as shown in Figure 10-3. Figure 10-4 shows the AN/UYK-20 central ORTS computer and its data base, as well as its interfaces with the AEGIS weapons system. Data Acquisition Converters (DACs) are used to develop the interfaces between the equipment and the data bases. Figure 10-5 lists the ORTS performance requirements. ORTS essentially has to detect all faults. The fault isolation requirements in the specification are that 95 percent of the faults will be processed either automatically or semi-automatically to reach the designation of an LRU, without additional test equipment. A functional view of ORTS/AEGIS is shown in Figure 10-6. The circled

items are considered to be BIT functions. The ORTS system is considered a macro-BITE within the AEGIS system.

The AN/SPY-1A/ORTS test configuration is displayed in Figure 10-7. Of the 181.2K core in the SPY-1 computer, approximately ten percent is devoted to the self-testing function. A total of 4,500 test points are examined through the 47 DACs, including 178 on-line detection tests. The AN/UYK-20 ORTS computer program uses about 52K words of core with another 25K non-core resident. ORTS files are shown, indicating the relative sizing, totalling roughly 10 to 12 percent of the tactical system. The tactical disk storage capability is 20 M words. ORTS uses 2 to 2.5 words total.

Figure 10-8 shows a typical maintenance sequence. The initial fault detection comes from the system AN/UYK-7 computers. Evaluation is performed by the AN/UYK-20 ORTS computer. Fault detection and identification outputs of ORTS are shown.

AEGIS/ORTS was installed in 1973 on the USS Norton Sound for evaluation and test firings. Prior to this, RCA built a replica of the Norton Sound deck house, called the Land Based Test Site (LBTS). The same Navy crew operating the LBTS was sent to the Norton Sound to conduct the tests. Presently, RCA has another facility at Moorestown representing the AEGIS cruiser deckhouse that has been operating for two years. The Norton Sound crew is presently operating, testing and debugging this facility and will go to the first AEGIS Cruiser, the USS Ticonderoga. Tests are controlled by the Combat System Maintenance Central (CSMC) including test conduct, personnel schedule, deferred maintenance, etc., providing central control for all maintenance.

A third facility has been constructed at Moorestown for test and checkout of the production AEGIS, using ORTS in the

system verification process. It can test two AEGIS production systems at a time.

The verification approach and ORTS requirements are shown in Figure 10-9. "One-on-one" represents the cabinet-to-DAC interface which was developed at the RCA Burlington facility and at Raytheon. The 178 on-line detection tests may sample 10 to 20 test points at a time to determine the operation of a function. Some fault isolation tests may run from 20 to 300 pages of flow charts for a single diagnostic test on a single cabinet. The test plan must include all ORTS testing to determine the percentage of equipment tested (including ORTS). A good data collection system is required to correlate ORTS design with actual failures. A "Trouble and Failure Report" has been developed by the Navy and RCA to provide supplementary failure reporting for AEGIS. The CSMC aboard ship also includes a representative of RCA.

Tools and methods used in design and evaluation of ORTS are shown in Figure 10-10. Special data base utility programs allow the modification of parameter values and tolerances to accommodate design changes. The Utility to Save and Restore the Disk (USAR) utility program permits taking the data base from the disk and putting it on magnetic tape. It can later be loaded on disk, if required. This capability permits test coordination among different test teams at different locations. The on-line radar test puts 35 32-bit words into the ORTS I/O buffer, telling the SPY-1 radar to perform certain actions. The return from this radar is 27 32-bit words. This sequence is termed a "test dwell." It is on-line and is interleaved with the operational dwells on a non-interruptive basis. Interruptive radar tests are held to a minimum.

Operational Test Definition and Criteria are shown in Figure 10-11. Fault ID numbers are on the order of 15,000 to 20,000 different numbers.

Things to verify are shown in Figure 10-12. Operational performance is achieved by utilizing the same people that are going to operate the system in the fleet.

Integration and test phasing of ORTS are shown in Figure 10-13. I&CO tests are qualitative, while O&P and performance tests are quantitative. The diagram represents a time period of 24 to 26 months.

The status of ORTS integration and checkout is shown in Figure 10-14. It is expected to be completed by the end of the year. Conclusions reached as a result of the Aegis/ORTS Program are shown in Figure 10-15.

DISCUSSION POINTS

- A Test Requirements and Analysis (TRA) group was established to receive test requirements from the various design engineers prior to incorporating them in the test plan for fault detection and fault isolation.
- Two test teams were used for a period of two years; each team (of three to six persons) was at the site four hours per day to complete testing of the EDM system.

Figure 10-1

THE REAL WORLD OF OPERATIONAL AVAILABILITY

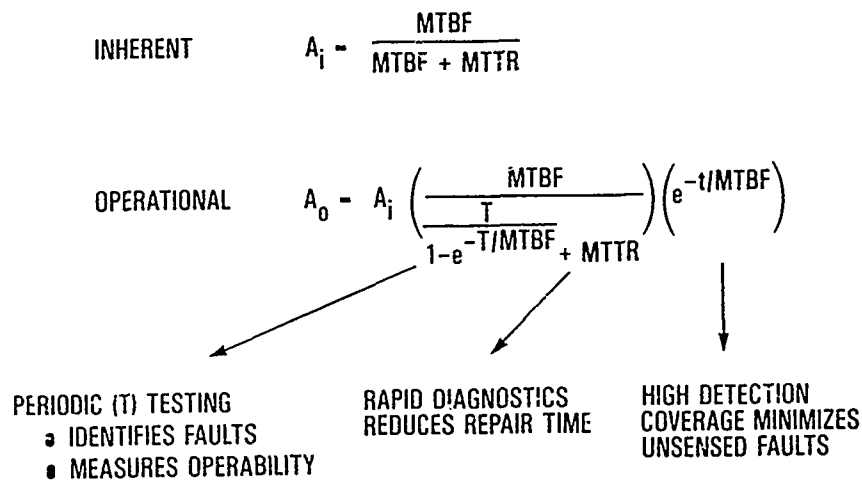


Figure 10-2

THE SYSTEM DESIGN PROCESS

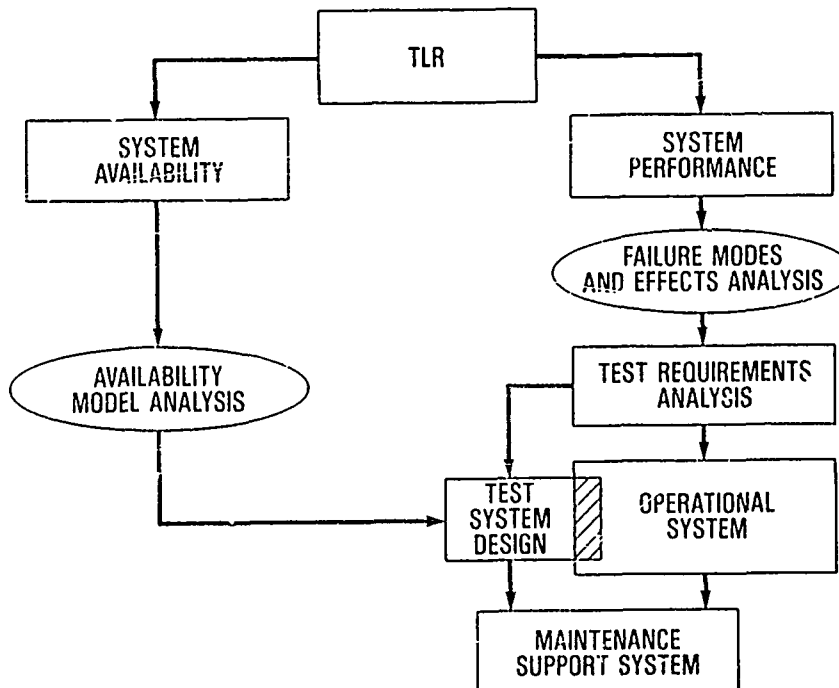


Figure 10-3

ALLOCATION OF AWS REQUIREMENTS FOR ORTS

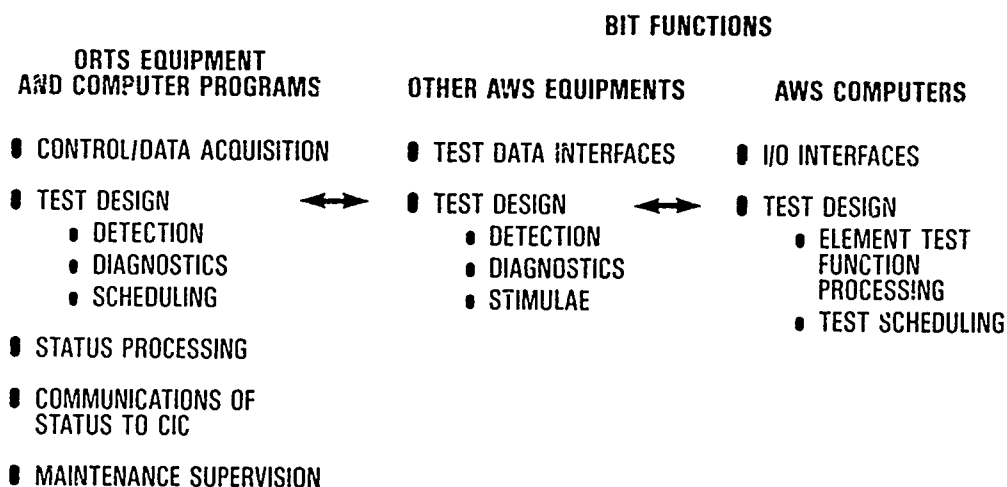


Figure 10-4

AEGIS/ORTS EQUIPMENT CONFIGURATION

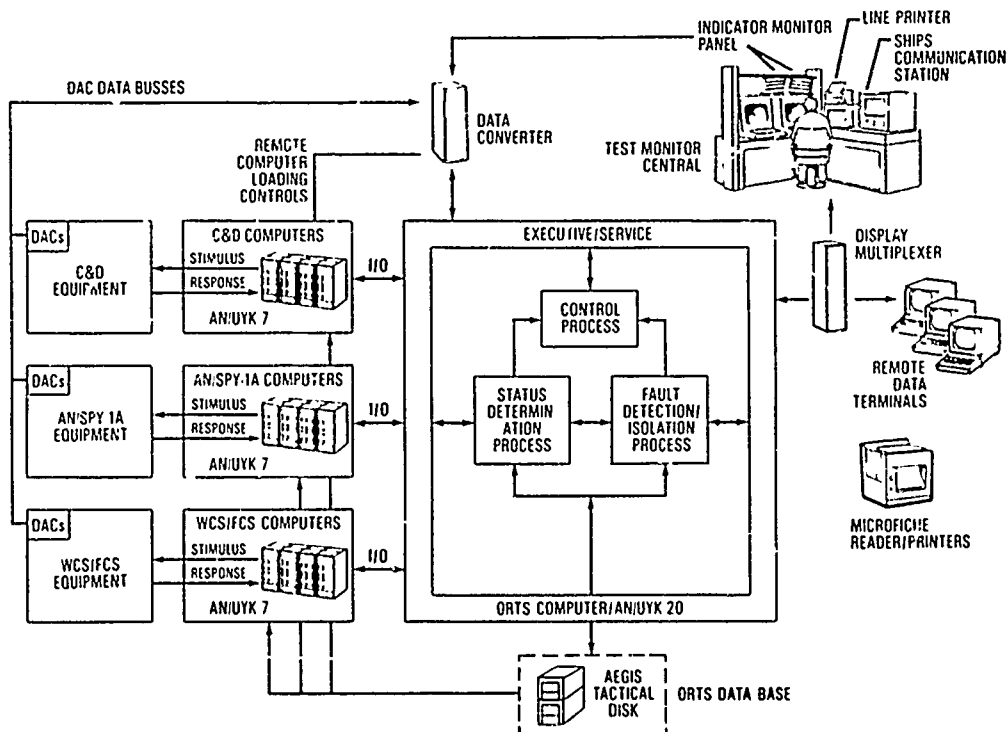


Figure 10-5

AEGIS/ORTS PERFORMANCE REQUIREMENTS

- DETECT FAULTS — EQUIPMENT, FUNCTIONS, MODES
- INTERPRET CHANGES OF STATUS
- FAULT ISOLATE AND COORDINATE MAINTENANCE
- INTERFACE WITH SHIPS LOGISTICS SUPPORT SYSTEM

Figure 10-6

ORTS/AEGIS WEAPON SYSTEM TEST DATA PROCESSING

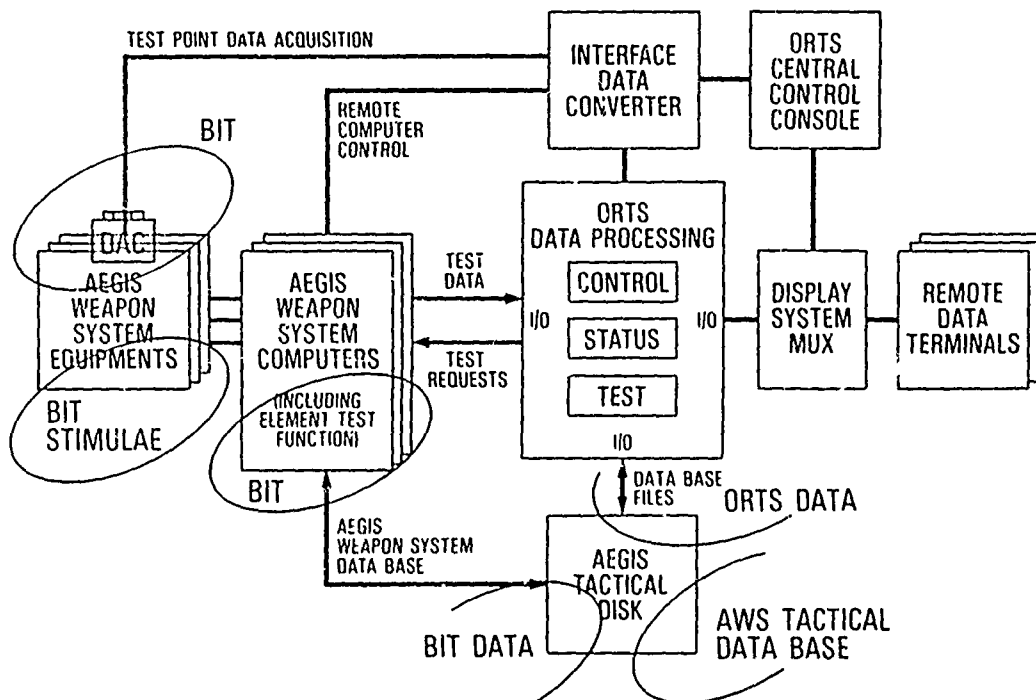


Figure 10-7

AN/SPY-1A/ORTS TEST CONFIGURATION

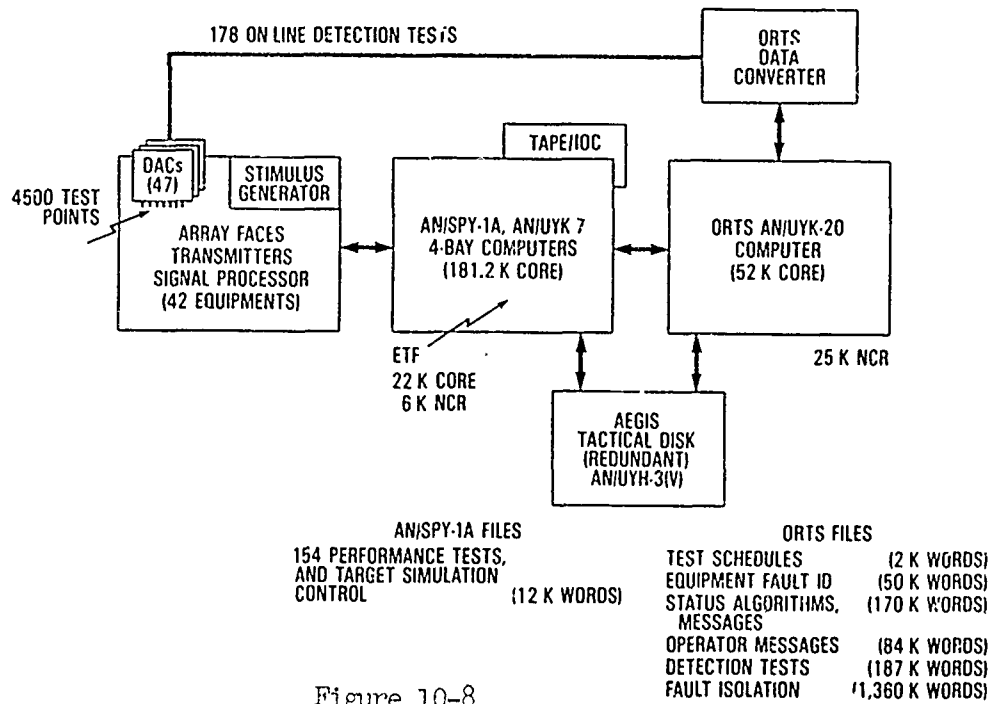


Figure 10-8

THE DIAGNOSTIC/CORRECTIVE MAINTENANCE SEQUENCE

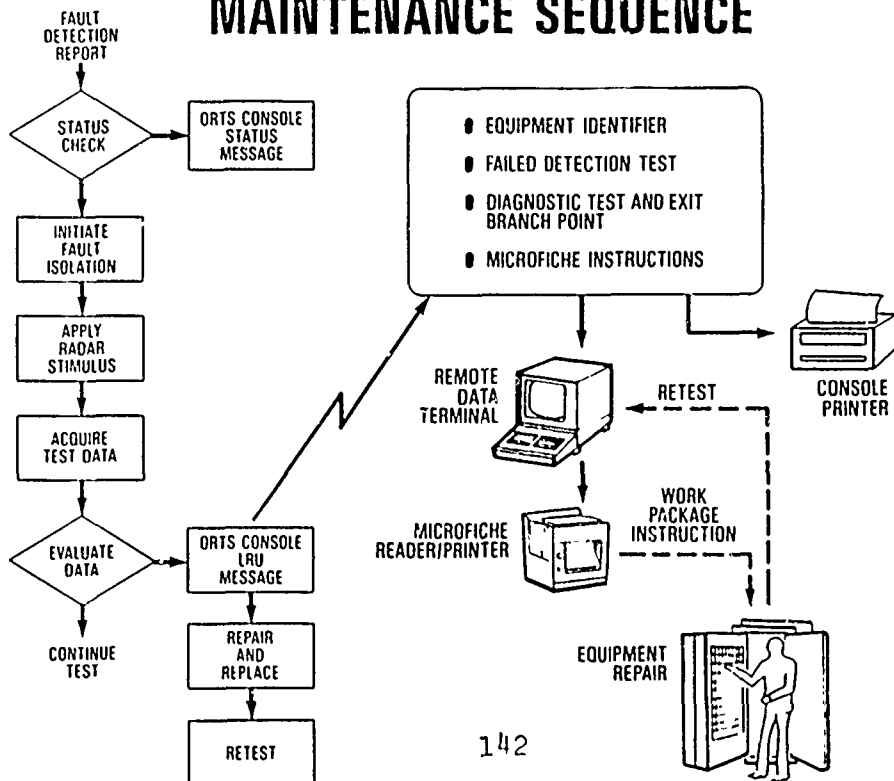


Figure 10-9

VERIFICATION APPROACH — ORTS REQUIREMENTS

- ORTS VERIFICATION IS A CONTINUAL PROCESS
- USE ORTS EARLY IN THE TESTING PROCESS
- USE "ONE-ON-ONE" INTEGRATION PLAN
- CONCENTRATE INITIAL EFFORT ON FAULT DETECTION TESTS
- ESTABLISH TOOLS/METHODS TO VERIFY TEST DESIGN
- USE ORTS CAPABILITY INCREMENTALLY
- CORRELATE ORTS TEST DESIGN WITH ACTUAL FAILURES

Figure 10-10

TOOLS/METHODS

- TECHNICAL REVIEWS; DESIGN AND IN PROCESS
- PAPER ANALYSES
- COMPUTER PROGRAM DEBUG/UTILITY MODULES
- SPECIAL DATA BASE UTILITY PROGRAMS
- SPECIAL OPERATOR CONTROLLED TEST STIMULI COMMANDS
- SOFT FAULT INSERTION
- HARD FAULT INSERTION
- MAG TAPE DATA RECORDING AND REDUCTION
- DATA COLLECTION AND ANALYSIS

Figure 10-11

OPERATIONAL TEST DEFINITION/CRITERIA

- TEST EXECUTES/CYCLES AND IS EXECUTABLE IN SEMI-AUTO AND AUTO-SCHEDULE MODE
- GO PATH VERIFIED; DISPLAYS, ALERTS, MESSAGES, DATA/TEST RESULTS, STATUS PROPAGATION, etc.
- NO GO PATH VERIFIED; DISPLAYS, ALERTS, MESSAGES, DATA INSERTION, STATUS PROPAGATION/DISPLAYS, FAULT RESULT ID NUMBER, AND AUTO DETECTION TO ISOLATION LINKS
- FAULT RESULT ID NUMBER LINK TO MICROFICHE ADDRESS FOR REPAIR/REPLACEMENT INSTRUCTIONS

Figure 10-12

THINGS TO VERIFY

- ORTS OPERATIONS AND INTERFACES
 - ORTS EQUIPT/COMPUTER PROGRAM/DATA BASE PROCESSING "MECHANISMS"
 - TEST POINT AND INTER-COMPUTER CHANNEL INTERFACES
- TESTS/TEST DESIGN VERIFICATION
 - TEST EXECUTION/OPERABILITY
 - TEST RESULTS/MEASUREMENT CREDIBILITY
 - OPERATIONAL PERFORMANCE

Figure 10-13

INTEGRATION AND TEST PHASING

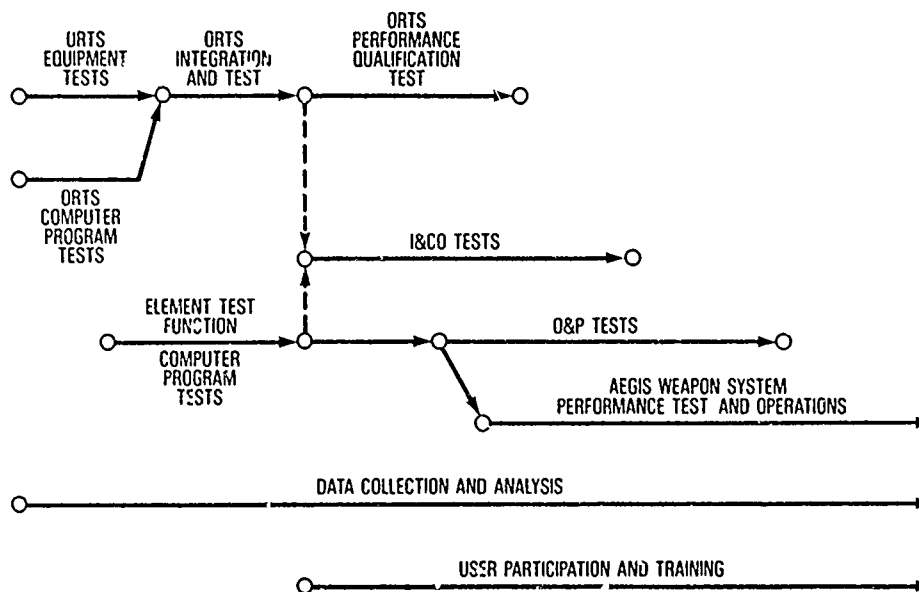


Figure 10-14

ACCOMPLISHMENT/STATUS

- ORTS OPERATIONS QUALIFIED AND WORKING
- ALL TEST POINT CHANNEL INTERFACES IN AEGIS ARE OPERATIONAL
- INTER-COMPUTER CHANNEL INTERFACES (AN/UYK-20 TO AN/UYK-7 SUITES) ARE OPERATIONAL
- AN/SPY-1A TEST/TEST DESIGN VERIFICATION STATUS
 - 122 OF 178 ON-LINE SCANS (OLS) ARE OPERATIONAL
 - 98 OF 154 ETF OPERATIONAL PERFORMANCE TESTS (OPTs) ARE OPERATIONAL
 - 27 OF 83 FAULT DETECTION/ISOLATION TESTS ARE OPERATIONAL
- ORTS BEING USED DAILY BY BOTH RCA AND NAVY FOR TEST AND MAINTENANCE

CONCLUSIONS

- VERIFICATION OF BIT FUNCTIONS IN AEGIS IS A COMPLEX BUT ACHIEVABLE PROCESS
- INTEGRATION AND TEST IS A CONTINUING, PLANNED, ACTIVITY
- IN AEGIS, *AVAILABILITY* HAS DRIVEN BIT
 - REQUIREMENTS
 - DESIGN
 - VERIFICATION
 - OPERATIONAL EVALUATION
- A DEGREE OF DESIGN ADAPTABILITY IS REQUIRED
- THE NAVY USER MUST CRITIQUE, PARTICIPATE, AND TRAIN *WITH* THE SYSTEM AS ITS OPERATIONAL CAPABILITY EVOLVES

BIT SPECIFICATION AND DEMONSTRATION TECHNIQUES

Captain Dan Gleason
RADC

Captain Gleason is the
Maintainability Design
Engineer for the RADC

HIGHLIGHTS OF THE PRESENTATION

Some of the problem areas discovered by RADC in certain exploratory development (6.2 funding category) studies were: unnecessary removals, high false alarm rates, and low fault isolation and fault detection percentages. A 30 to 40 percent RTOK rate was found quite universal. RADC awarded a contract to Hughes Aircraft to perform a field survey to investigate and verify the RTOK problem, document RTOK rates and determine a means to minimize removals. Nine aircraft types, six equipments, twelve bases and two repair facilities were included in the survey. Definitions used are shown in Table 1 of the attachment (excerpted from the study report).

The main results of the study are indicated in Figure 11-1. Primarily it was found that maintenance personnel in the field had to resort to "unseemly" troubleshooting practices. Since they sometimes don't know where the problem is, they resort to indiscriminate removals of boxes. In addition, there is a "horizontal testability" problem where a unit will test "good" at one AIS and "bad" at another AIS at the same facility. Easy accessibility as required for most LRUs encourages indiscriminate removals. In some cases, adjacent boxes require one to be removed in order to obtain access to the latches on the other box. In this case, both boxes are frequently sent back to the shop. Depot practices of cleanup prior to testing and repair may result in the removal of the fault (e.g. dirty connector) during cleanup and the consequent RTOK. Inconsistencies were found in filling out the 349

forms and transferring information to the 350 tags among bases. All maintenance actions are pilot driven and sometimes pilots report failures that don't exist.

The study results also showed a mean value of 38 percent for unnecessary removal rates which ranged from 4 percent to 89 percent for different equipment LRUs. Sometimes, unnecessary adjustments are made at the I-level shop in order to avoid a maintenance event being termed an unnecessary removal, possibly resulting in the numbers shown being conservative.

Study of the false alarm problem included the equipments shown in Figure 11-2 for the data base. Categories of false alarms included Category I, a system failure but an isolation to the wrong box, and Category II, the classic false alarm where there is no failure in the system but BIT says there is. False alarm rates for the F-15 radar systems and the F-14 radar systems, respectively, were: F-15 AN/APG-63 Category I--38 percent, Category II--22 percent; F-14 AN/AWG-9 Category I--28 percent, Category II--53 percent, where the percentage is the percent of fault indications.

Fault isolation problems on the S-3A aircraft are shown in Figure 11-3, based on a study by Lockheed. Actual fault isolation percentages to the SRU level all fall far short of design percentages. This indicates that maintenance personnel are not being given enough assistance. Severe turnaround time requirements sometimes force the removal of three or four boxes instead of isolating to one box. Removal and checkout of one box at a time requires more aircraft down time.

Results of an ASD study of several avionic equipments are shown in Figure 11-4; the results are summarized for the four less successful equipments. These results show a direct correlation between the number of fault detections and the number of false alarms declared. In addition to the equipment's shown, the AN/ARC-164 showed the same relationship.

In this case, the BIT detection capability in the ARC-164 was reduced and the false alarm rate also decreased. No loss in operational capability was observed as a result of this decrease. Overspecification (e.g. 99 percent detection, one percent false alarm rate) is a contradiction that does not appear possible to achieve at the present time.

Objectives of the RADC Figure of Merit (FOM) Study are shown in Figure 11-5. Specific BIT objectives are categorized in Figure 11-6. A survey of industry resulted in the FOM list shown in Figure 11-7. These FOMs are associated with fault detection capability in Figure 11-8 and with fault isolation capability in Figure 11-9. The most significant physical and operational characteristics affecting BIT are shown in Figure 11-10.

Analysis and demonstration techniques applicable to each FOM are shown in Table 2 of the Attachment; some of these techniques are summarized in Figures 11-11, 11-12, and 11-13. RADC has a joint program with the Naval Electronics Systems Command (Washington, D.C.) to develop improved methods of maintainability prediction to supplement or replace some of the procedures in MIL-HDBK-472 addressing BIT capabilities. It is presently being circulated for comments. BIT suitability factors were included in the industry survey and addressed the factors shown in Figure 11-14. They were ranked in accordance with their suitability to meet the specification objectives shown in Figure 11-15. The BIT FOM selection process used in the study is shown in Figure 11-16 for each candidate FOM. Results of selection of BIT FOMs are summarized in Table 6 of the Attachment.

The maintenance concept objective to improve flight line efficiency by removing only the one failed LRU and to improve I-level efficiency by removing only the one failed SRU. Calculations were performed to determine how many removals can be

expected for each system failure. The methodology used in these calculations is shown in Figure 11-17. In this figure, X is a measure of fault isolation capability, $P(MA)$ is the probability of missed assignment (erroneous fault indication), and RR is removal rate (which is dependent upon maintenance policy).

A typical example of ENR (expected number of removals) calculations is provided in Figure 11-18, showing 141 boxes removed for every 100 failures in an instance when single unit removal maintenance policies were used. Under conditions of a group removal policy, the number becomes 177 boxes removed for every 100 failures.

Requirements for logistic specifications are shown in Figure 11-19. Logistic specification FOM relationships to costs are shown in Figure 11-20. ENR is relatable to Mean Time Between Removal (MTBR). It is measurable, traceable and relates directly to life cycle costs.

FOM conclusions and recommendations are shown in Figure 11-21.

The methodology to apply a MIL-STD-471 demonstration is shown in Figure 11-22. Figure 11-23 shows the deficiencies in this methodology today. For example, if the SPO is not adequately monitoring the selection of the failure population, FMEAs are sometimes not performed, hazardous failures are not identified, and failure samples may not be randomly selected. In addition, the MIL-STD-471 demonstration is performed in a sterile environment and does not reflect field conditions.

UNNECESSARY REMOVALS

FINDINGS TO DATE

FACTORS THAT CONTRIBUTE TO UNNECESSARY REMOVALS

- o BUILT-IN-TEST
- o TEST EQUIPMENT
- o TECHNICAL ORDERS
- o MAINTENANCE PROCEDURES
- o TRAINING
- o ACCESSIBILITY
- o MAINTENANCE CONCEPTS
- o DEPOT PRACTICES
- o DATA COLLECTION

Figure 11-1

FALSE ALARM PROBLEM

- o RADC CONTRACTUAL EFFORT WITH HUGHES AIRCRAFT SUPPORT SYSTEMS GROUP
- o ANALYSIS OF BIT FALSE ALARMS CONDITIONS
 - 1. FUNDAMENTAL CAUSES AND FREQUENCY
 - 2. DESIGN GUIDELINES
 - 3. PREDICTION FACTORS
- o DATA BASE
 - 1. AN/APG-63 FIRE CONTROL RADAR (F-15)
 - 2. AN/AWG-9 RADAR & WEAPONS CONTROL (F-14)
 - 3. TPO-37 ARTILLERY LOCATING RADAR (ARMY)

Figure 11-2

FAULT ISOLATION PROBLEM

S-3A

	DESIGN %			ACTUAL %		
	1SRU	2SRU	3SRU	1SRU	2SRU	3SRU
ANALOG	88	98	100	41	63	78
DIGITAL	81	96	100	37	58	73
RF	86	98	100	42	62	76
POWER SUPPLY	91	97	100	55	74	92

Figure 11-3

FAULT DETECTION PROBLEM

	FAULT DETECTION (%)	FALSE ALARM (%)
TACAN	48	0
AN/APN 185	54	14
AN/APN 190	30	10
AN/AYK-6	91	38-50

BIT FOM SPECIFICATION & DEMONSTRATION

OBJECTIVES

- o BIT/EXTERNAL TEST FIGURES OF MERIT AND DEMONSTRATION TECHNIQUE (RADC-TR-79-309),
- o SURVEY & INVESTIGATE CURRENT MEASURES AND FIGURES OF MERIT (FOM) USED TO SPECIFY BUILT-IN-TEST (BIT) AND EXTERNAL TESTER (ETE) ADEQUACY.
- o DETERMINE METHODS OF MEASUREMENT AND DEMONSTRATION FOR THE FOMs.
- o PROVIDE GUIDANCE AS TO HOW TO SPECIFY THESE FOMs.
- o PROVIDE GUIDANCE FOR INTEGRATION OF BIT/ETE REQUIREMENTS, ANALYSIS, AND DEMONSTRATION INTO CURRENT MAINTAINABILITY PROGRAM PLANS.

Figure 11-5

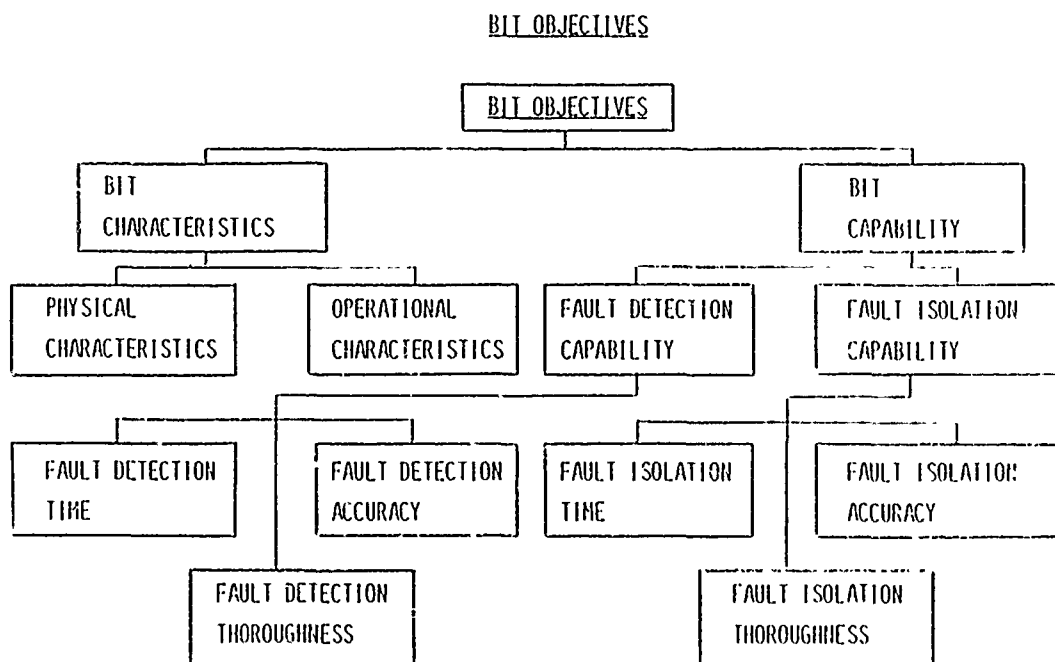


Figure 11-6

GENERALIZED FOHS

1. FRACTION OF FAULTS DETECTED (FFD)
2. FRACTION OF FALSE ALARMS (FFA).
3. FRACTION OF FALSE STATUS INDICATIONS (FFSI).
4. MEAN FAULT DETECTION TIME (T_{FD}).
5. MEAN BIT RUNING TIME (T_B).
6. FREQUENCY OF BIT EXECUTIONS (F_B).
7. TEST THOROUGHNESS (TT).
8. FAULT ISOLATION RESOLUTION (FIR(L)).
9. FRACTION OF FAULTS ISOLATED (FFI).
10. MEAN FAULT ISOLATION TIME (T_{FI}).
11. MAINTENANCE PERSONNEL SKILL LEVEL (MPSL).
12. BIT MAINTAINABILITY (HTTR_{B/E}).
13. BIT RELIABILITY (MTBF_{B/E}).
14. BIT AVAILABILITY (A_{B/E}).
15. EQUIPMENT AVAILABILITY (A).
16. EQUIPMENT MAINTAINABILITY (HTTR).
17. FRACTION OF FALSE PULLS (FFP)
18. FRACTION OF ERRONEOUS FAULT ISOLATIONS (FEFI)

Figure 11-7

BIT OBJECTIVES

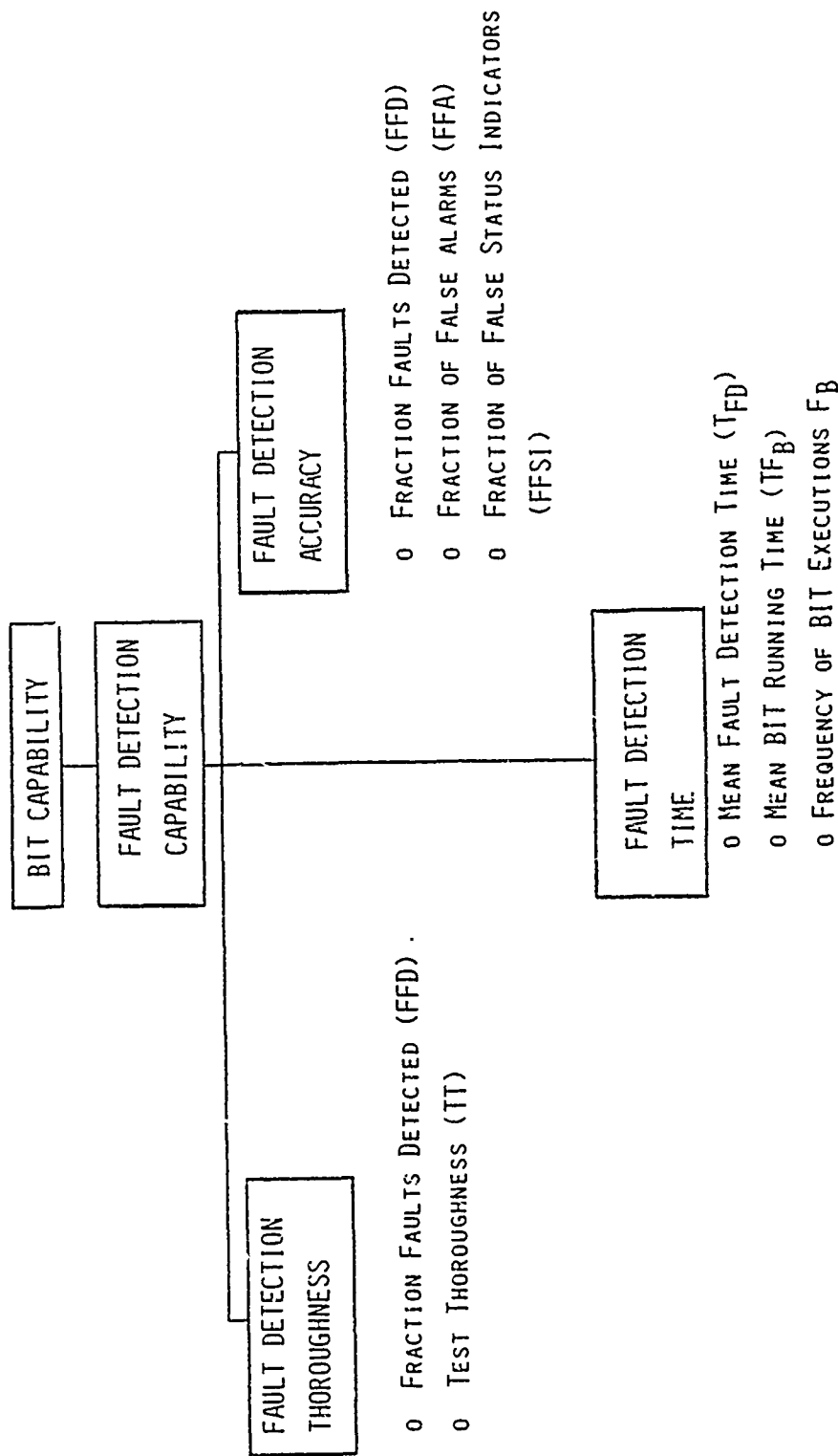


Figure 11-8

BIT OBJECTIVES

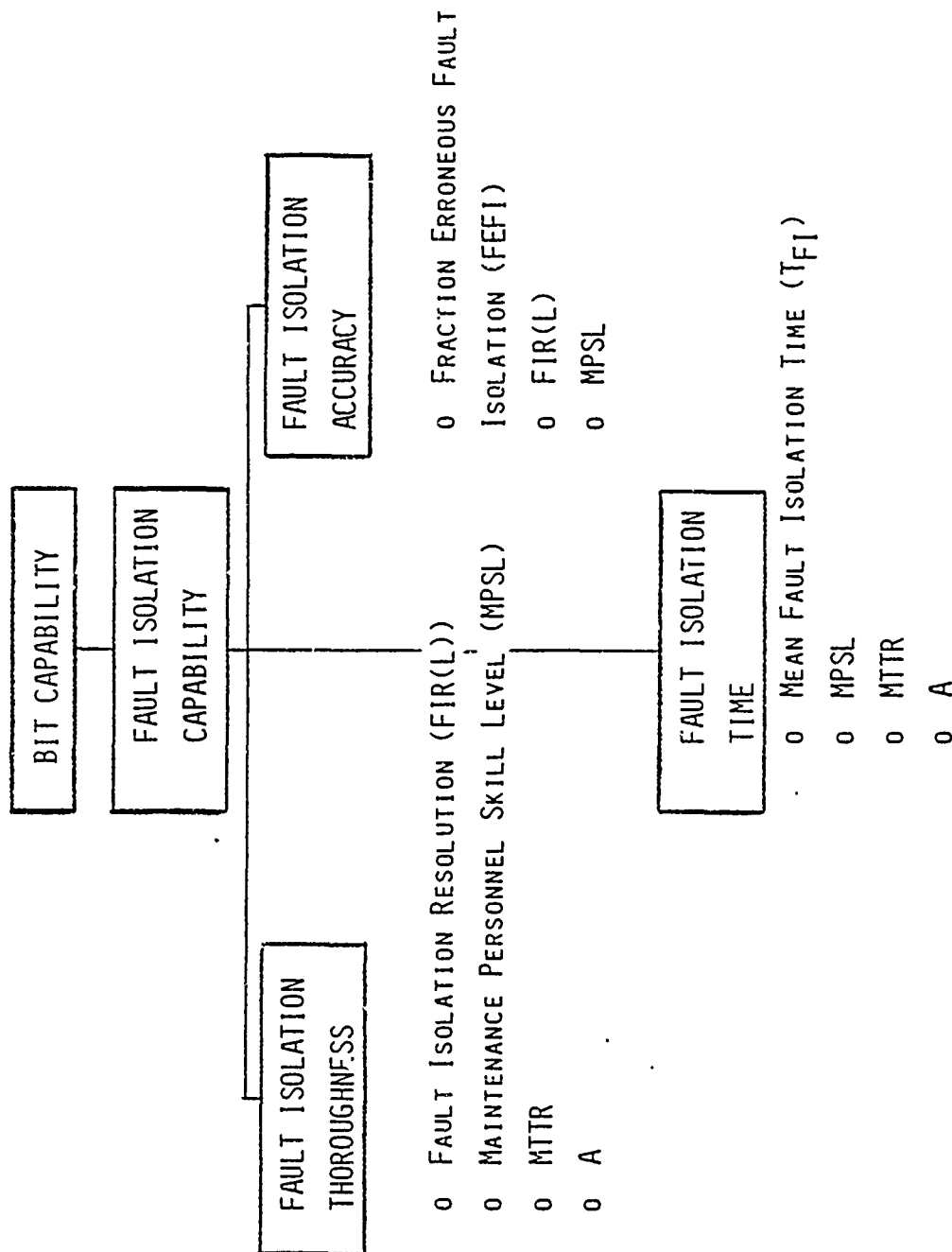


Figure 11-9

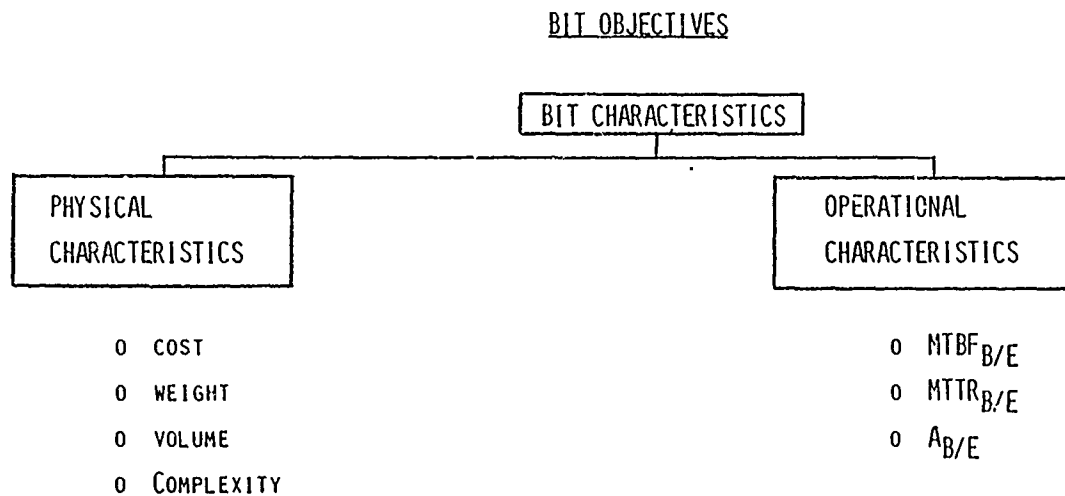


Figure 11-10

BIT FOM SPECIFICATION & DEMONSTRATION

<u>FOM</u>	<u>ANALYSIS TECHNIQUE</u>	<u>DEMONSTRATION TECHNIQUE</u>
FFD	CAN BE ANALYZED BY A RATIO OF OCCURRENCE RATES (E.G., FAILURE RATE)	CAN BE VERIFIED BY A BINOMIAL DISTRIBUTION OR BY FIELD DATA COLLECTION
FFA	CAN BE ANALYZED BY A RATIO OF OCCURRENCE RATES (E.G., FAILURE RATE)	CAN BE VERIFIED BY FIELD DATA COLLECTION ONLY
FFSI	CAN BE ANALYZED BY A RATIO OF OCCURRENCE RATES (E.G., FAILURE RATE)	CAN BE VERIFIED BY FIELD DATA COLLECTION ONLY
\bar{T}_{FD}	CAN BE ANALYZED BY A METHOD SIMILAR TO MIL-HDBK-472 PROCEDURE 2 OR RADC-TR-78-169, A FAILURE RATE WEIGHTED AVERAGE OF TIMES (TIMES DETERMINED THRU TIME LINE ANALYSIS)	CAN BE VERIFIED BY DIRECT TIME MEASUREMENT

Figure 11-11

BIT FOM SPECIFICATION & DEMONSTRATION

BINOMIAL TEST TABLES

(FFD, FEFI, TT, FFI)

FIND PROBABILITY OF PASSING A TEST AS A FUNCTION OF THE TRUE FOM VALUE FOR FIXED n AND k .

FIND n AND k WHERE DESIGN FOM GOAL, MINIMUM FOM ACCEPTABLE, AND CONSUMER AND PRODUCERS RISKS ARE GIVEN.

FIND DESIGN FOM GOAL, MINIMUM FOM ACCEPTABLE, AND CONSUMER AND PRODUCERS RISKS FOR GIVEN n AND k .

WHERE n = SAMPLE SIZE

k = PASS/FAIL CRITERIA

Figure 11-12

BIT FOM SPECIFICATION & DEMONSTRATION

MULTINOMIAL DISTRIBUTION

FIR(L)

TYPICALLY EXPRESSED AS MULTIPLE REQUIREMENTS

DEMONSTRATE

1. SPECIFY MINIMUM ACCEPTABLE CRITERIA
2. SPECIFY CONSUMER/PRODUCER RISK
3. DERIVE TEST STATISTIC (T) AND TEST CRITERIA (C)

PRODUCER PASSES IF $T \geq C$

Figure 11-13

BIT FOM SELECTION PROCESS

SUITABILITY FACTORS

1. UNIQUENESS
2. TRACKABILITY
3. DEMONSTRATABILITY
4. TRANSLATABILITY
5. AMBIGUITY
6. APPLICABILITY

Figure 11-14

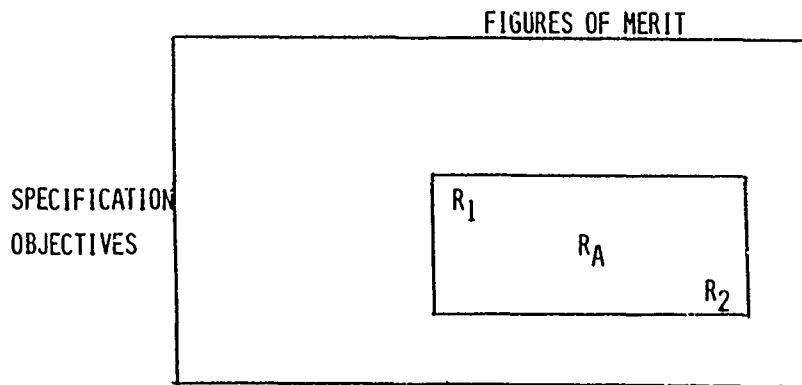
BIT FOM SELECTION PROCESS

SPECIFICATION OBJECTIVES

1. CONTINUOUS PERFORMANCE
2. ACCURATE STATUS REPORTING
3. MINIMUM DOWNTIME
4. LIMITED SPARES
5. MINIMUM SUPPORT COSTS
6. SPECIFIC SKILL LEVELS
7. SYSTEM LOCATION
8. BIT INTEGRAL TO SYSTEM
9. ON-LINE TESTING LENGTH/PERIODICITY
10. SOFTWARE TESTING LIMITATIONS
11. UNDETECTED FAILURES
12. BIT OPERABILITY/ACCURACY
13. PHYSICAL AMOUNT OF BIT

Figure 11-15

BIT FOM SELECTION PROCESS



R_1 - RANKING DUE TO SUITABILITY FACTORS

R_2 - RANKING DUE TO SPECIFICATION OBJECTIVE

R_A - AVERAGE RANKING

Figure 11-16

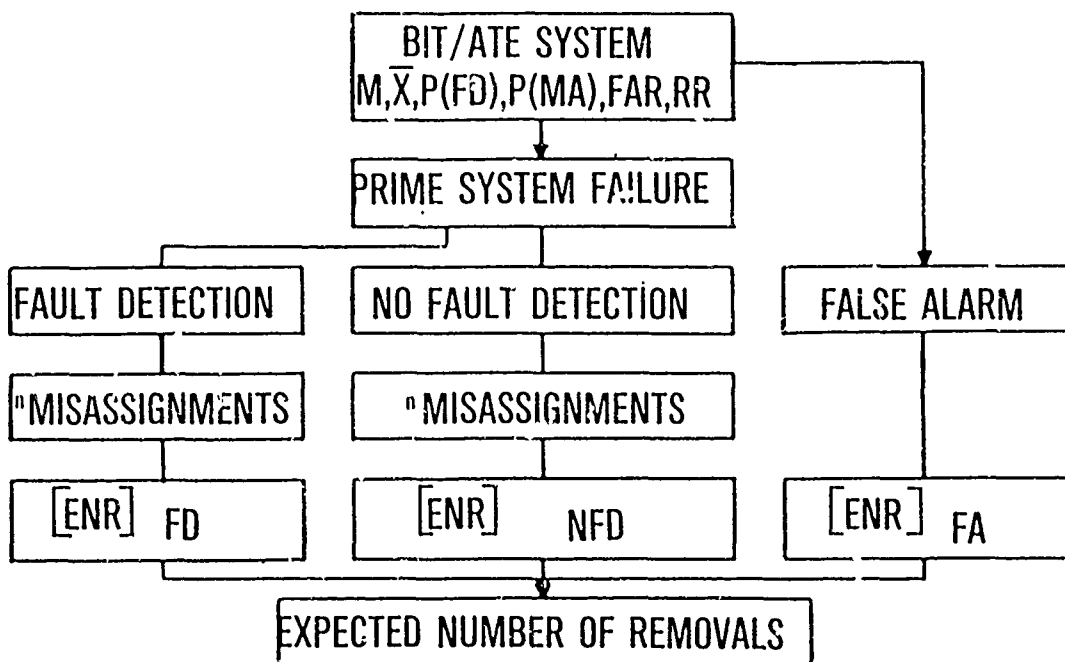


Figure 11-17

$$\text{ENR} = \frac{\text{EXPECTED NUMBER OF REMOVALS}}{\text{SYSTEM FAILURE}}$$

EXAMPLE

$$M = 5 \qquad P(\text{MA}) = .05$$

$$\bar{X} = 1.07 \qquad \text{FAR} = .05$$

$$P(\text{FD}) = .90$$

$$\text{ENR} = 1.41$$

Figure 11-18

LOGISTIC SPECIFICATIONS

SPECIFIC REQUIREMENTS

1. FAULT DETECTION
2. FAULT ISOLATION
3. ERRONEOUS FAULT INDICATIONS

GENERAL REQUIREMENTS

1. REMOVALS PER FAILURE
2. FALSE PULL RATE
3. MTTR

Figure 11-19

LOGISTIC SPECIFICATION

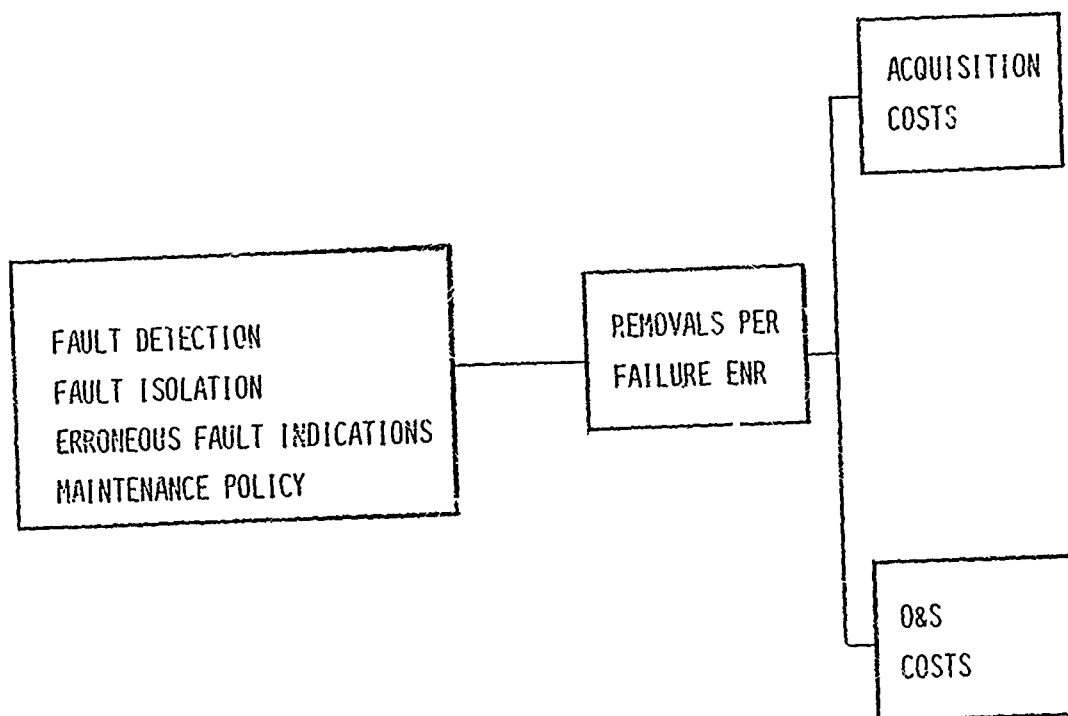


Figure 11-20

CONCLUSIONS/RECOMMENDATIONS

CURRENT FOMs ARE ADEQUATE IF PROPERLY DEFINED

FOMs CAN BE GENERAL OR SPECIFIC

FOMs CAN BE SPECIFIED WITH MINIMUM IMPACT ON CURRENT MAINTAINABILITY PROGRAMS

1. MIL-STD-470
2. MIL-STD-471

Figure 11-21

471 DEMONSTRATION

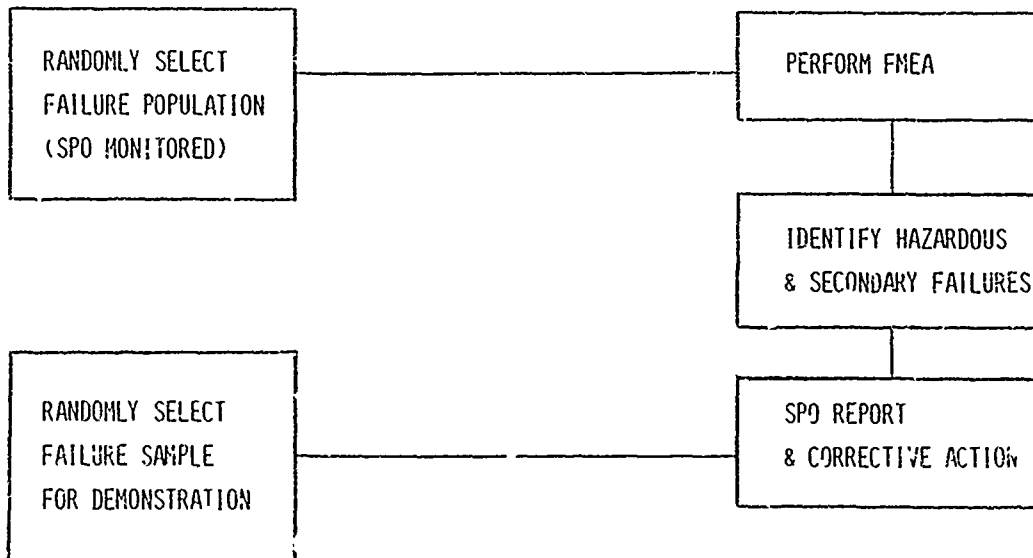


Figure 11-22

471 DEMONSTRATION

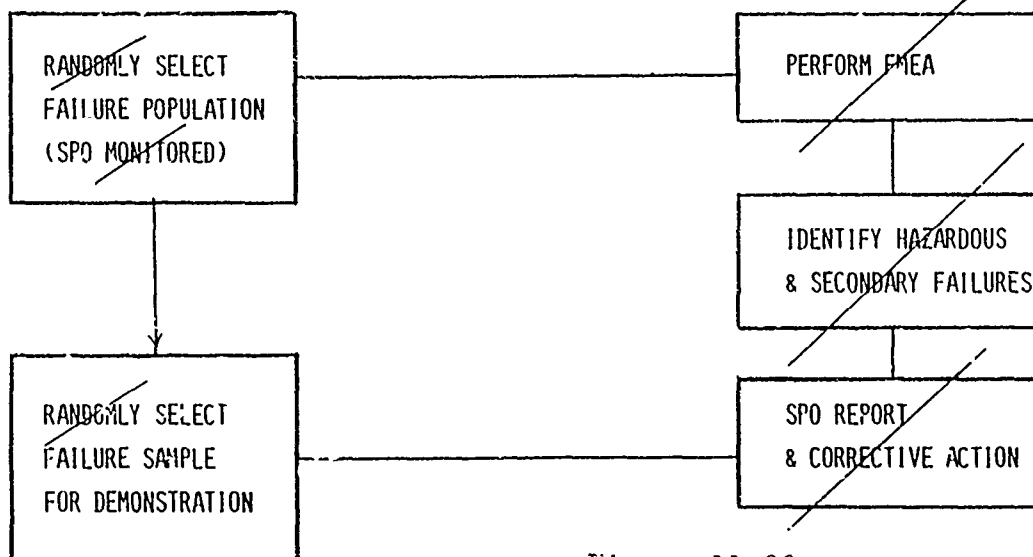


Figure 11-23

BUILT-IN-TEST SPECIFICATION
& DEMONSTRATION TECHNIQUES

(ATTACHMENT)

CAPT DANIEL GLEASON
R&M ENGINEERING SECTION
ROME AIR DEVELOPMENT CENTER

#	Figure of Merit	Definition	General Model	
1	Fraction of Faults Detected (FFD)	a) the fraction of all faults detected (or detectable) by BIT/ETE. b) the fraction of all detectable faults detected (or detectable) with BIT/ETE.	$FFD_A = \frac{\text{quantity of faults detected by BIT/ETE } (Q_{BDE})}{\text{quantity of all faults } (Q_F)}$ $FFD_D = \frac{\text{quantity of faults detected by BIT/ETE } (Q_{BDE})}{\text{quantity of faults detected } (Q_{FD})}$	
2	Fraction of False Alarms (FFA)	the fraction of all BIT/ETE indicated faults which are false alarms. False alarms are those indications of a fault when an actual fault has not occurred.	$FFA = \frac{\text{quantity of BIT/ETE false alarms } (Q_{FA})}{\text{quantity of all BIT/ETE indicated faults } (Q_{BIF})}$	
3	Fraction of False Status Indications (FFSI)	The fraction of BIT/ETE fault indications (or lack thereof) which are erroneous.	$FFSI = \frac{\left\{ \begin{array}{l} \text{quantity of} \\ \text{false alarms } (Q_{FA}) \end{array} \right\} + \left\{ \begin{array}{l} \text{quantity of undetected} \\ \text{faults } (Q_{UD}) \end{array} \right\}}{\left\{ \begin{array}{l} \text{quantity of BIT/ETE} \\ \text{indicated faults } (Q_{BIF}) \end{array} \right\} + \left\{ \begin{array}{l} \text{quantity of undetected} \\ \text{faults } (Q_{UD}) \end{array} \right\}}$	
4	Mean Fault Detection Time (T_{FD})	The average time it takes for BIT/ETE function to detect and indicate a fault from the time the fault has occurred.	$T_{FD} = \frac{Q_{BDF}}{\sum_{i=1}^n (\text{time to detect and indicate the } i^{\text{th}} \text{ BIT/ETE detectable fault})}$	
5	Mean BIT/ETE Running Time (T_B)	The average active time to perform a BIT/ETE routine. This can be the average for one test, a group of tests, or all tests.	$T_B = \frac{NB}{\sum_{i=1}^n (\text{active running time of the } i^{\text{th}} \text{ BIT/ETE test routine, } T_{B_i})}$	
6	Frequency of BIT/ETE Executions (F_B)	The frequency (or cycling rate) at which periodic BIT/ETE tests are executed (This does not apply to BIT/ETE tests that are executed only upon requests).	$F_B = \frac{\left\{ \begin{array}{l} \text{the time it takes to execute the complete set of BIT/ETE} \\ \text{test routines} \end{array} \right\} + \left\{ \begin{array}{l} \text{the idle time between the execution of the complete} \\ \text{set of BIT/ETE test routines} \end{array} \right\}}{-1}$	
7	Test Thoroughness (T_T)	The fraction of the equipment/system tested by BIT/ETE relative to the entire equipment/system.	$T_T = \frac{\text{(amount of system/equipment tested by BIT/ETE)}}{\text{(amount of system/equipment tested by BIT/ETE)} + \text{(amount of system/equipment not tested by BIT/ETE)}}$	
8	Fault Isolation Resolution (FIR(L))	The fraction of detected faults isolated by BIT/ETE down to an acceptable (specified) minimum number of replaceable items.	$FIR(L) = \frac{\text{quantity of detected faults isolatable to } \leq L \text{ RUs with BIT/ETE } (Q_{IL})}{\text{quantity of detected faults } (Q_{FD})}$	
9	Fraction of Faults Isolated (FFI)	The fraction of faults detected by BIT/ETE, isolated with BIT/ETE to the replacement level specified by the maintenance concept.	$FFI = \frac{\text{quantity of detected faults isolated with BIT/ETE } (Q_{IB})}{\text{quantity of faults detected } (Q_{FD})}$	
10	Mean Fault Isolation Time (T_{FI})	The average time to complete the fault isolation process using BIT/ETE.	$T_{FI} = \frac{Q_{BDF}}{\sum_{i=1}^n (\text{time to isolate the } i^{\text{th}} \text{ fault with BIT/ETE})}$	

Table 1. SUMMARY OF DEFINITIONS

(cont'd)

11	Maintenance Personnel Skill Level (MPSL)	a) the average skill level required to perform corrective maintenance for a system/equipment b) the minimum skill level required to perform corrective maintenance on a system/equipment	Not Applicable
12	BIT/ETE Reliability (MTBF _{B/E})	The probability that the BIT/ETE circuitry will perform its intended function for a specified interval under specified conditions. BIT/ETE circuitry is any hardware that is used for BIT/ETE testing that is not common to the system hardware.	$MTBF_{B/E} = \lambda_{B/E}^{-1} = \left\{ \sum_{k=1}^{NB/E} \lambda_{B/E_k} \right\}^{-1}$ $NB/E = \text{quantity of BIT/ETE hardware components not common to system hardware}$
13	BIT/ETE Maintainability (MTTR _{B/E})	The average time to repair a fault in the BIT/ETE hardware.	$MTTR_{B/E} = \frac{\sum_{k=1}^{NB/E} \lambda_{B/E_k} MCT_k}{\sum_{k=1}^{NB/E} \lambda_{B/E_k}}$
14	BIT/ETE Availability ($\lambda_{B/E}$)	A measure of the degree to which the BIT/ETE circuitry is in the operable and committable state at the start of a mission, when the mission is called for at an unknown (random) point in time.	$\lambda_{B/E} = \frac{MTBF_{B/E}}{MTBF_{B/E} + MTTR_{B/E}}$
15	System Maintainability (MTTR)	The average corrective maintenance time for all system/equipment faults.	$MTTR = \frac{\sum_{i=1}^N \lambda_i M \alpha_i}{\sum_{i=1}^N \lambda_i}$
16	System Availability (A)	A measure of the degree to which a system/equipment is in the operable and committable state at the start of a mission, when the mission is called for at an unknown (random) point in time.	$A = \frac{MTBF}{MTBF + MTTR}$
17	Fraction of False Pulls (FFP)	The fraction of RIs removed from a system, due to the result of a BIT/ETE fault isolation process, that are good RIs (i.e., RIs with no actual failure within it).	$FFP = \frac{\text{quantity of good RIs removed } (Q_{GRI})}{\text{quantity of RIs removed } (Q_{RR})}$
18	Fraction of Erroneous Fault Isolation Results (FEFI)	The fraction of BIT/ETE fault isolation results that identify the wrong RI once a fault has been detected.	$FEFI = \frac{\text{quantity of erroneous fault isolation results, } (Q_{EFIR})}{\text{quantity of fault isolation results, } (Q_{FIR})}$

Table 1 Concluded

BIT/ETE FOM	Analysis Technique	Demonstration Technique
<ul style="list-style-type: none"> Fraction of Faults Detected (FFD) Fraction of False Alarms (FFA) Fraction of False Status Indications (FFSI) Mean Fault Detection Time (T_{FD}) Mean BIT/ETE Running Time (T_B) Frequency of BIT/ETE Executions (F_B) Test Thoroughness (TT) Fault Isolation Resolution (FIR (L_i)) Fraction of Faults Isolated (FFI) Mean Fault Isolation Time (T_{FI}) Maintenance Personnel Skill Level (MPSL) 	<ul style="list-style-type: none"> can be analyzed by a ratio of occurrence rates (e.g., failure rate) can be analyzed by a ratio of occurrence rates (e.g., failure rate) can be analyzed by a ratio of occurrence rates (e.g., failure rate) can be analyzed by a method similar to MIL-HDBK-472 procedure 2 or RADC-TR-78-169, a failure rate weighted average of times (times determined thru time line analysis) can be analyzed by time line analysis since there is no randomness in its occurrence can be analyzed by time line analysis since there is no randomness in its occurrence can be analyzed by a ratio of occurrence rates (e.g., failure rate) can be analyzed by a ratio of occurrence rates (e.g., failure rate) can be analyzed by a ratio of occurrence rates (e.g., failure rate) can be analyzed by a method similar to MIL-HDBK-472, procedure 2 or RADC-TR-78-169, a failure rate weighted average of times (times determined thru time line analysis) can be analyzed by a weighted average of skill levels if it is defined as an average, otherwise it is strictly determined by measuring the maximum skill level required for each maintenance action can be analyzed using MIL-HDBK-217 	<ul style="list-style-type: none"> can be verified by a binomial distribution or by field data collection (FFD only) can be verified by field data collection only can be verified by field data collection only can be verified by direct time measurement can be verified by direct time measurement can be verified by direct time measurement can be verified by direct measurement or the same way FFD is demonstrated, depending on how it is defined can be verified by a multinomial distribution or by field data collection can be verified by a binomial distribution or by field data collection can be verified by techniques similar to MIL-STD-471 or by field data collection can be verified by direct measurement or by field data collection can be verified by using the techniques of MIL-STD-781 or field data collection can be verified using the techniques of MIL-STD-471 or field data collection can be verified by using the techniques of MIL-STD-781 and MIL-STD-471 or by field data collection can be verified by using the techniques of MIL-STD-471 or field data collection can be verified by using the techniques of MIL-STD-781 and MIL-STD-472 or by field data collection can be verified by a binomial distribution or by field data collection
<ul style="list-style-type: none"> BIT/ETE Reliability (MTBFR/E) BIT/ETE Maintainability (MTTRB/E) BIT/ETE Availability (A_B/E) System Maintainability (MTTR) System Availability (A) Fraction of Erroneous Fault Isolation Results (FEFI) 	<ul style="list-style-type: none"> can be analyzed using MIL-HDBK-217 can be analyzed using MIL-HDBK-472, RADC-TR-78-169 can be analyzed using current techniques to determine reliability and maintainability (e.g., MIL-HDBK-217, MIL-HDBK-472, etc...) can be analyzed using MIL-HDBK-472, RADC-TR-78-169. can be analyzed using current techniques to determine reliability and maintainability (e.g., MIL-HDBK-217, MIL-HDBK-472, etc...) can not be analyzed 	<ul style="list-style-type: none"> can be verified by using the techniques of MIL-STD-781 or field data collection can be verified using the techniques of MIL-STD-471 or field data collection can be verified by using the techniques of MIL-STD-781 and MIL-STD-471 or by field data collection can be verified by using the techniques of MIL-STD-471 or field data collection can be verified by using the techniques of MIL-STD-781 and MIL-STD-472 or by field data collection can be verified by a binomial distribution or by field data collection

Table 2. SUMMARY OF BIT/ETE FOM ANALYSIS/DEMONSTRATION TECHNIQUES

REQUIREMENT	FFD	FFA	FFSJ	TFD	TB	FB	TT	FIR(L)	FII	TFI	MPSL	MTDF BIT	MTTR BIT	Λ _{BIT}	MTR	A	FMAD	FEI
1) CONTINUOUS PERFORMANCE	2	6	5	4	3	3	5									1		
2) ACCURATE REPAIRS/REPAIRING	1	4	3	6			5					2	2					
3) MINIMUM DOWNTIME					7			4	3	7	6		5		1	2		8
4) LIMITED SPARES								1										
5) MINIMUM SUPPORT COSTS		4	5					1	2									3
6) SKILL LEVELS SEE NOTE 2	1						7	3	4	6	5				2			6
7) SYSTEM LOCATION								1										2
8) BIT/ETE INTEGRAL TO SYSTEM		3	2									1						
9) ONLINE TESTING LEAD TIME/PERIODICITY					2	1												
10) SOFTWARE TESTING LIMITATIONS																	1	
11) UNDETECTED FAILURES	1		3	2			3											
12) BIT/ETE OPERABILITY/ACCURACY		5	4									1	2	3				
13) PHYSICAL AMOUNT OF BIT/ETE									SEE NOTE 3									

NOTES

1. FOR THE AVERAGE RANKING, IF TWO OR MORE FOMS HAD THE SAME AVERAGE RANK, THE FOM THAT HAD THE HIGHER RANK FROM THE BIT/ETE EVALUATION WAS RANKED HIGHER.
2. FOR SYSTEMS THAT REQUIRE A SPECIFIC SKILL LEVEL TO MAINTAIN A SYSTEM, MPSSL SHOULD BE SPECIFIED. THE OTHER FOMS LISTED CAN BE USED TO IMPOSE REQUIREMENTS THAT ARE DUE TO THE MPSSL REQUIREMENT.
3. FOR SYSTEMS THAT DESIRE THIS OBJECTIVE, THE BIT/ETE FOM THAT CHARACTERIZES THE PHYSICAL LIMITATION SHOULD BE SPECIFIED.

Figure 6. Correlation of RMA and BIT/ETE Objectives with the Defined BIT/ETE FOMs

BIT WORKSHOP PANELS

Martin Meth
OSD, MRA&L

Mr. Meth is the Staff
Engineer for OSD, MRA&L.

Three panels have been formed for the purpose of discussing perceived major issues involving BIT. Each panel is asked to identify what is currently being done, and what could be done to resolve some of the identified problems in the near, intermediate and long term. The three panels address the problems: how do we specify BIT, how do we do development tests, and how do we do operational test.

The Requirements Panel will address the questions of how the user, the operator, and the program people define a set of requirements against which we should design BIT and other diagnostics. How should manpower and readiness questions be taken into account (broadly scoping these requirements, including the resources required to support system development). In the past, poor planning (including not setting aside test articles) has resulted in schedules being grossly underestimated. It appears that more thinking and planning should be done during the requirements phase.

The Subsystem Panel will address the questions of how we specify requirements for equipments such as radars, how we do the development testing, and the design verification to determine that what we specify is actually built into the equipments. In other words, what should we tell the contractor, what should we expect back from him in terms of response, and what we expect in terms of design validation.

The System Panel will address the questions of how we specify requirements on the system given that we have a lot of equipments comprising the system, how we do system design verification, and how we operationally test the system to see that the requirements have been met.

Panel members have been arbitrarily selected. The three panels will present (tomorrow morning) half-hour reports including problem statements, observations and recommendations; from this we may arrive at a consensus of whether there are answers to certain problems and, if there are, what those answers are most likely to be. Recommendations for present alternatives and for future research should be included.

Each panel has been provided with one copy of all the vu-graphs, for reference, as well as a copy of all the homework comments turned in by the workshop members. Panels will meet for approximately two hours this afternoon.

The question has been raised as to whether another BIT Workshop would be appropriate which would deal with specific methods and techniques for implementation of BIT (since this present workshop deals with certain management aspects of BIT such as specification, verification and testing of BIT). Recommendations from the three panels are requested. Although the scope of such a workshop may be extended to include other BIT subjects, specific BIT implementation would probably be the primary, and possibly the only, subject of the workshop.

Many programs underway today appear to be repeating many of the mistakes of past programs. It is important that the messages of this workshop get to the people running these programs to avoid compounding these mistakes. Panel recommendations are requested in this area.

DISCUSSION POINTS

- It is apparent that many people in the BIT community are not aware of the existence of pertinent documents

such as some RADC BIT evaluation reports. Those interested in being put on the RADC distribution list should contact Dan Gleason or Tony Coppola.

- An Automatic Testing Newsletter is published by NAVMAT (George Neumann). It can be used to advise the BIT community of the existence of various reports. (At the present time, many of the people in the BIT community do not receive that newsletter.)
- Other newsletters exist that might contain information of benefit to the BIT community such as AFSC, IEEE Reliability Society, AAE, and ASQC.
- The tri-service JLC annual meeting is being held in September, 1981 in San Diego. Participation by members of the BIT community would be appropriate to further exchange information.

INSTRUCTIONS TO THE GROUPS

Summarize for each issue or observation the major problems and proposed solutions. The following should be considered as the issues are addressed:

(1) Does the group agree that the statements of issues and observations are within the defined scope? If not, add to or change, as appropriate.

(2) Characterize the issues and observations in terms of degree of criticality, anticipated ease or difficulty of resolution, and priority for resolution.

(3) Identify whether the problems associated with each issue and observation are technical or managerial.

(4) In describing the solutions, discuss the adequacy of what is currently being done to resolve the problems; what changes should be immediately implemented. What could be accomplished in the next two years, five years and how should these changes be implemented. Also discuss what specific parts of the acquisition process (e.g., specifications, procedures) need to be changed and suggest changes.

(5) Define the BIT terms used in the group discussion.

(6) Identify research areas that should be pursued to improve the specification, test and evaluation of BIT.

GROUP #1 REQUIREMENTS Wessel (Leader)

Geret	Drummond
Nunn	Bragg
Walters	Charles
Shafer	Dudek
Griffith	Shebell

GROUP #2 SUBSYSTEMS Keiner (Leader)

Linden	Schumacher
Faggard	Meyer
Cappola	Victor
Jenkins	Chen
Towsen	Harrison
Kauffman	

GROUP #3 SYSTEMS Gleason (Leader)

Danforth	Boardman
Vershish	McCarthy
John Rogers	Pyle
Gunkel	Pontious
Pruitt	Wilson
England	

REQUIREMENTS AND EFFECTIVENESS (GROUP #1)

Scope: Statement of Program BIT requirements; relationship of BIT requirements to maintenance capability as well as broader operational needs; evaluation of tradeoffs between BIT requirements and other related program requirements--test equipment, personnel skills, spares.

Issues/Observations: The relationship between BIT performance and operational needs for logistics and manpower requirements are not well understood.

1. In what terms should program BIT requirements be expressed--broad maintenance diagnostic terms? BIT contract specifications or both? How should the BIT requirements be related to operational needs? (a) Operational needs encompass indications to the system operator that the system is operating satisfactorily and (b) the capability to find system failures and return to operational status to meet system availability or usage requirements.

2. What should be the process for formulating the program BIT requirement ?

a. Who should be responsible for developing these BIT requirements?

b. When should the BIT requirements be developed?

c. What tradeoffs need to be considered in developing BIT requirement and related personnel skills, test equipment, and spares requirements.

Issues/Observations: Inadequate resources and unrealistic schedules are being proposed for development of BIT.

1. What should be the process to determine if the program BIT requirements are realistic or achievable?

2. How should program funding and development schedules be estimated for BIT development? What factors should be considered--test facilities, test articles, etc.

SUBSYSTEM AND SPECIFICATION TESTING (GROUP #2)

Scope: Equipment which is part of a major system; new or existing design; BIT requirements for contracts; validation of BIT for contractual compliance; evaluation of BIT performance on maintenance capability and operational needs.

Issues/Observations: The results of contractor BIT demonstrations (using fault insertions) do not match BIT performance in the field.

1. How should BIT requirements be specified in a subsystem contract? What specific terms should be used? Should the specifications include both quantitative measures (i.e., percent faults detected) and design guidelines (i.e., partitioning of functions)?

2. Should different BIT terms be specified in contracts for different types of equipment? Different mechanizations?

Issues/Observations: Analysis of BIT design efforts are not providing data to determine if BIT specifications can be met.

1. What type of design data and analysis should the subsystem contractor use to manage the BIT design/development efforts? What data should be provided to and by the system contractor?

2. How should the contractor demonstrate compliance with BIT contractual requirements prior to subsystem delivery? Should BIT demonstrations include both analysis and testing? What should be the specific "deliverables" by the contractor.

What are the limitations of contractor BIT demonstrations? What test areas need improvement? (Considerations--fault selection approach and sample size).

3. What other tests that are usually performed during subsystem development can be used in the determination of BIT contractual compliance.

4. How can the subsystem contractor get visibility of subsystem BIT field performance at the level of detail required to find and fix deficiencies?

Issues/Observations: Funding and schedule allocated for BIT development are generally not adequate.

1. What type of analysis needs to be completed prior to contracting to show that the specified BIT performance values are feasible and achievable.

2. How should the funding, design and test schedules, test facilities and articles be estimated for the BIT subsystem development?

SYSTEM REQUIREMENTS AND TESTING (GROUP #3)

Scope: Systems or equipment used in the military operations; integration of subsystems into system; specification of BIT requirements in contracts; demonstration of contractual compliance; operational test and evaluation of BIT.

Issues/Observations: Performance of BIT in the field is generally much lower than observed in testing prior to production.

1. What is the best way to communicate BIT performance requirements to the system developer?
2. How should BIT be specified in contracts? What specific terms should be used? Should the specifications include both quantitative measures (i.e., percent fault detected) and design guidelines.
3. How should the system contractor demonstrate compliance with the BIT specifications. Should compliance be demonstrated by tests, analysis or both.
4. What should be the operational test measures of BIT performance? How should these measures be related to BIT contract requirements, program BIT requirements?
5. What are the areas of BIT performance that cannot be evaluated until after the system is fielded?

Issues/Observations: Current approaches to BIT system design do not take into account many real world problems as evidenced by high levels of false alarms, undetected failure, retest ok's and ambiguities.

1. Should the BIT contract specifications for systems also include subsystem specifications? Should the subsystem allocation consider criticality (mission safety, etc.) feasibility and/or operational information measures. How should the subsystem/system interface requirements be specified?

2. What type of design data, testing, analysis should the system contractor use to manage the system and subsystem BIT design efforts? What data and analysis should be provided to the program office?

Issues/Observations: BIT performance in the field has not been compatible with planned personnel skills, test equipment, and other logistics.

1. How should requirements for skill level of personnel, test equipment and spares be included in the BIT specifications?

2. To what extent can BIT performance measured under operational test conditions be related to manpower requirements, test equipment performance and spares requirements?

Issues/Observations: Resources and schedule allocated for BIT development are generally not adequate.

1. What factors need to be considered in estimating whether the BIT contract requirements are realistic and achievable and that appropriate resources (funds, test assets, etc.) have been budgeted.

2. What ways can be used to combine contractor demonstration of BIT with field demonstrations to develop a sense of how well the BIT works.

BIT WORKSHOP PANEL NO. 1 REPORT:
REQUIREMENTS AND EFFECTIVENESS

PANEL CHAIRMAN: LT. COLONEL JIM WESSEL, USAF

Lt. Colonel Wessel is Chief
of the Logistics Assessment
Procedures Division of
AFTEC

HIGHLIGHTS OF THE PANEL REPORT

BIT performance vs operational needs is a problem which generally is not well understood--the Panel concensus was that this is a true statement. In fact, the operational user really does not have and should not specify BIT requirements in terms of traditional parameters, such as percentage of FD and FI.

The operational user's requirements should be in the form of sets of constraints consisting of such operational and maintenance parameters as turnaround time, maximum down time, manpower levels, skill levels, and self sufficiency in deployment. FD and FI should not be specified by the user. During the process of system definition, the optimum "diagnostic" system should be defined within the user constraints consisting of automatic and manual diagnostic capabilities (Figure 13-1). This system consists of BIT, people, T.O.s, and test equipment. The contractor and the procurer must then define the required diagnostic system identifying how much is automatic, how much is manual, and the percentages of FD and FI.

Figure 13-2 addresses the issue of the relationship of BIT requirements to operational needs. It is shown that there are two basic operational needs of the diagnostic system: fault detection for the operator and fault isolation for the maintainer. The operator needs fault detection to answer the questions: what have I got, what can I do, what don't I have, what can't I do. His needs for information are different from those of the maintainer. The operator does not need to know

which LRU is bad. He needs to be provided with mission-critical information. The maintenance person needs fault isolation in order to know which LRU is bad in order to repair it. The operational user should identify for the producer/contractor upfront what the information needs are for the operator and for the maintainer. Normally these needs are different.

Figure 13-3 addresses the issue of the requirements formulation process. The Panel consensus was that it is an interactive process between user and procurer and between procurer and contractor. The user and supporter (depot) should define their constraints; this should be done between Milestone 0 and Milestone 1 (preliminary operational concept). The diagnostics concept should be fairly well firmed-up by Milestone 1, but not totally defined at this point. The extent to which this can be done by Milestone 1 is questionable except for addressing higher level operational constraints. The trade-offs between performance requirements versus skill levels and between test equipment versus spares was not addressed in great detail. The Panel consensus was that tradeoffs were required in these areas, within operational and support constraints, to optimize the operational effectiveness of the weapon system. Sometimes the user must be told that his requirements cannot be met within the constraints allowed. Support constraints and life cycle costs have to be considered in context with performance requirements when tradeoffs are made. The procurer must make it clear to the contractor how requirements are specified and exactly what they mean in order for the contractor to determine how he is going to mechanize the system in terms of automatic and manual operation, test equipment, skill levels, etc. to meet user requirements. The key premise to the discussion is that the diagnostic system must provide 100 percent FD and 100 percent FI, although it is not all automatic. Tradeoffs between lower skill levels and smarter BIT, as well as tradeoffs

between fewer spares and more automatic test equipment, should be reasonably well determined by Milestone 1. What is implemented in the equipment itself needs to be determined by Milestone 2.

Figure 13-4 addresses the issue that inadequate resources and unrealistic schedules are being proposed for system development. The consensus of the Panel is that this is a true statement. Determination of whether the BIT requirements are realistic and achievable does not present a problem if development of the diagnostic system is considered a systems engineering discipline as related to all other ILS elements. If that is recognized, development of the diagnostic system with its BIT support should be the same kind of process as required to get reliability and maintainability into the system. A diagnostic development program is required, including a program plan. The system may include the imposition of ATE interface requirements such as with the MATE concept. The BIT program, with established milestones, assists in the evaluation of the realism of forecast BIT achievements.

Figure 13-5 addresses the issue of how to estimate funding and schedules. This issue was not addressed by the Panel because of time limitations. My opinion is that if the diagnostic discipline is defined and implemented as are other disciplines, funding and schedule requirements for diagnostics will be addressable as are those in the other development disciplines. The items listed in Figure 13-5 are those which should be considered in this area.

DISCUSSION POINTS

- By not recognizing the differences between operator FD information requirements and maintainer FI information requirements too much information may be given to the operator who may then be interpreting it incorrectly and possibly forcing more maintenance than would otherwise be necessary. On the other hand, in

some cases too little information may be provided the operator in terms of "what can I do" relative to completion of the mission.

- By Milestone 1, higher level constraints (e.g. whether there is any 0-level test equipment) should be resolved, permitting the contractor to determine how he's going to implement that requirement in the design.
- Differences exist between how the contractor evaluates his system and how the user evaluates it. For example, in the F-16, the 100 percent fault detection seen by the contractor was seen as 83 percent by the user.
- Every contractor has stated that he needed a dedicated test bed or dedicated time on a test bed and a long period of time in order to debug and mature the BIT.
- The concept of BIT flexibility to change and to accommodate changes and unforeseen events is important in BIT design. This flexibility must be designed upfront to accommodate transitions from development through production phases.
- Schedule requirements to mature current BIT systems indicate that roughly two years are required after the system is fielded to mature the BIT. This requires a maintenance evaluation team dedicated to gathering data on how well the diagnostics functions and sorting out where the problems are (hardware, software, test equipment, manuals, etc.). Prior to being fielded, the BIT had passed some military demonstration requirements.
- No attempt has been made to document the cost and schedule requirements necessary to mature the BIT in existing systems for use in projecting requirements for future systems. A knowledge base has not been developed in this area to determine what data to collect.
- If a BIT program has not been implemented from the very beginning, it is usually impractical and cost prohibitive to do so after the fact.
- Design for testability must become as much a part of the design discipline as design for performance presently is. Dedicated test articles and dedicated time in the test program assist in attaining this objective.
- The MATE concept (a system engineering discipline), if imposed as a test interface in a system such as the

Multi-Role Radar (MRR), will enforce a diagnostics design discipline. If it is not imposed, a proliferation of test equipment will result.

- Cost estimates for acquisition and test of supportability elements of the system are estimated at 20 percent of the system acquisition costs. BIT costs are included in this amount.
- F-18 cost estimates for BIT are seven percent of the hardware and 14 percent of the software costs. Development and validation of the design is an interactive process.
- More effective utilization of testbeds is essential to the future maturation of diagnostics.
- Limited 0-level support equipment should be considered as an alternative to no 0-level support equipment in some cases.

REQUIREMENTS & EFFECTIVENESS

ISSUE: BIT PERFORMANCE VS OPERATIONAL
NEEDS NOT WELL UNDERSTOOD

PROBLEM: TERMS FOR PROGRAM BIT REQUIREMENTS?

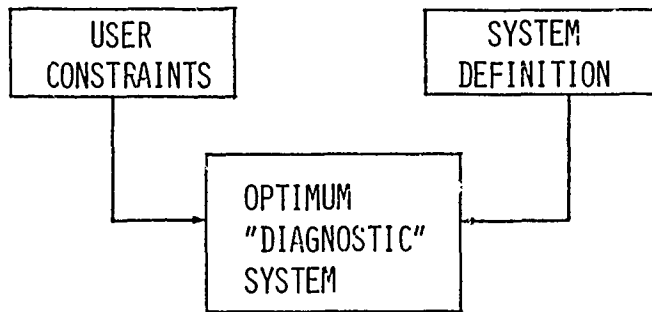


Figure 13-1

PROBLEM: BIT REQUIREMENTS VS OPERATIONAL NEEDS

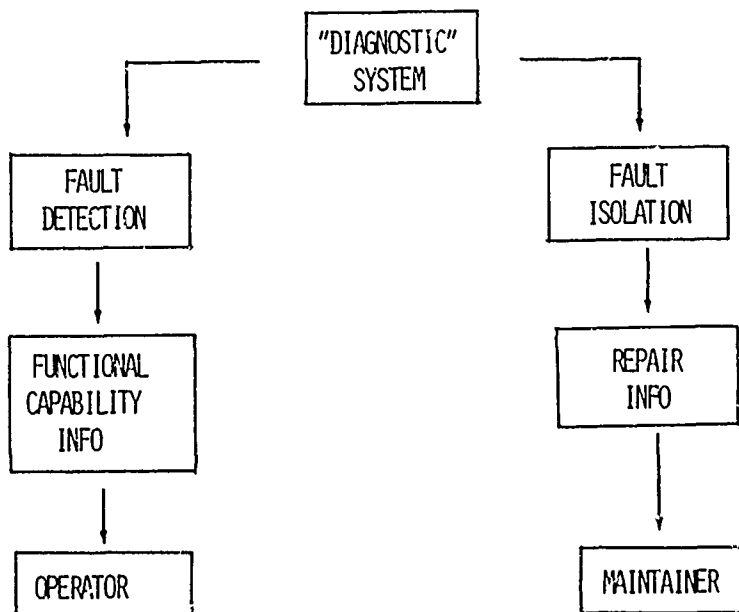


Figure 13-2

PROBLEM: REQUIREMENTS FORMULATION PROCESS?

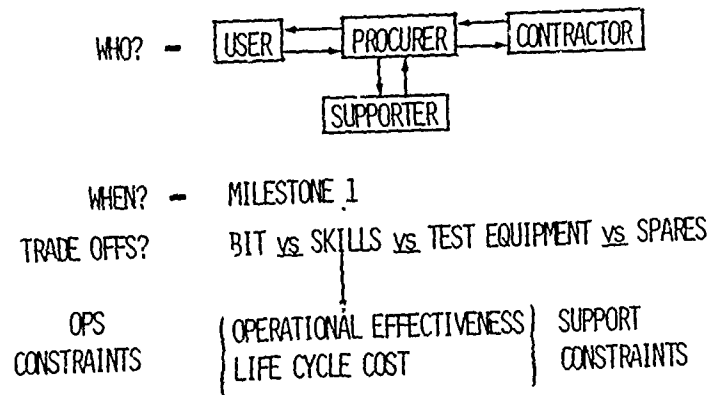


Figure 13-3

ISSUE: INADEQUATE RESOURCES & UNREALISTIC SCHEDULES
PROBLEM: PROCESS TO DETERMINE IF BIT RQMTS REALISTIC & ACHIEVABLE?

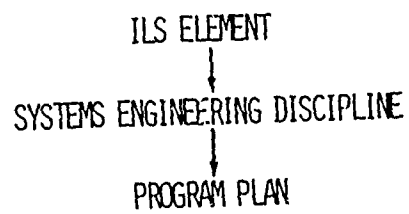


Figure 13-4

PROBLEM: HOW TO ESTIMATE FUNDING & SCHEDULES?

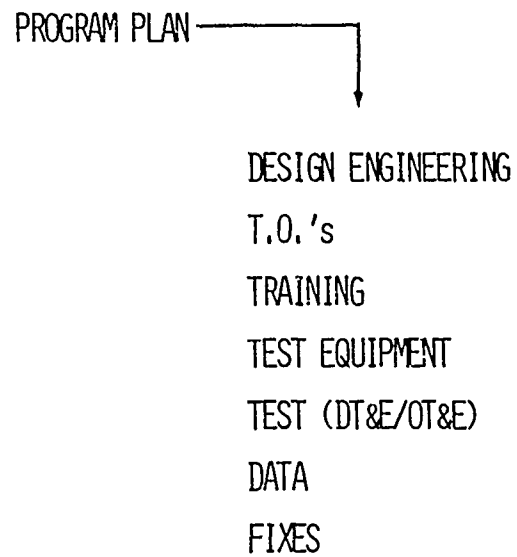


Figure 13-5

BIT WORKSHOP PANEL NO. 2 REPORT:
SUBSYSTEM BIT

PANEL CHAIRMAN: BILL KEINER

Mr. Keiner is the head of
the Testing Technology
Program Office at the NSWC

HIGHLIGHTS OF THE PANEL DISCUSSION

The four main points addressed by the Subsystem BIT panel were BIT design, specification, evaluation and management. Many of the conclusions of this panel are the same as those of the System Panel (No. 3) and won't be repeated here.

BIT design recommendations are shown in Figure 14-1. Decentralized (e.g., subsystems) BIT is recommended, maintaining flexibility to adjust thresholds and tolerances where possible. BIT processing technology ("smart BIT") should be developed further.

BIT specification recommendations are shown in Figure 14-2. Numerical BIT requirements should not be included in a MIL-STD; they should be derived for each system on an individual basis. Systems that include multiple-application subsystems (e.g., GFE) should have specification values for R&M that take into account previous experience with these subsystems.

BIT evaluation recommendations are shown in Figure 14-3. Early design analyses of BIT are essential to the development process. For example, in the case of VHSIC elements, BIT must be included at the time of initial circuit design. No opportunities are available for later incorporation.

Environmental tests should be combined with MIL-STD-471 tests to more clearly represent the operational environment and permit reduction of the post-development debugging time. More should be done to assure that the failure types demonstrated during factor acceptance testing represent those which occur

in the field (e.g., cable problems). Failure data relating to BIT performance should be collected during all types of testing.

BIT management recommendations are shown in Figure 14-4. BIT must take its proper place in the overall integrated diagnostic system.

DISCUSSION POINTS

- Adequacy and consistency of definitions is lacking, causing many communication problems in the BIT community; this problem does not appear to be adequately addressed at the present time. The BIT Design Guide includes some definitions, other definitions are included in RADC reports, but a comprehensive set of definitions is not available. A MIL-STD 1309C (Navy) will address BIT definitions.
- It appears that a single focal point for BIT should be established within system and subsystem contractors' facilities.
- Adequate management methods and motivation do not appear to exist at the present time (within government and industry) to implement guidelines and directive relating to BIT requirements.
- There does not appear to be a viable methodology to predict future BIT performance based on field experience with similar types of systems (e.g., F-18 and F-15).
- In one system, the BIT was very good and was used in factory acceptance testing and resulted in a saving of two percent of the recurring production cost because of reduced testing costs. Therefore, in some cases, early design for testability can actually save front-end acquisition dollars, rather than waiting for the payoff in long-term life cycle costs. However, data are generally not available to confirm this saving. These type of data should be collected to give proper management and design emphasis to testability.
- It is more efficient to use different types of testers during the design checkout phase since different types of failures are being sought (e.g. design errors) than those which occur during service use. However, the final tests in factory acceptance should be done with the BIT and ATE to be used in the field.

- Supportability must be included in initial design considerations to ensure that the system is supportable at the time of release for production. In the past, the supportability of systems has been "shoved under the rug" when considering the decision for release for production.
- The airlines are beginning to establish a data bank and central repository on BIT.
- The JLC Panel on Automatic Testing has established focal points in each of the Services for testability tasks.
- A "BIT Community" and a set of principles do not presently exist similar to the "Reliability Community". This should be established using newsletters as a vehicle for communications. This BIT Workshop effort should be continued to help organize this community.

BIT EVALUATION RECOMMENDATIONS

IMPLEMENT BIT AT SUBSYSTEM LEVEL

KEEP BIT DESIGN FLEXIBLE TO ALLOW BIT
MATURATION

EMPLOY INSTRUMENTATION
TO IDENTIFY INTERMITTENTS
TO ASSIST LATER TESTING

DEVELOP BIT PROCESSING TECHNOLOGY

CONSIDER DIFFERING NEEDS OF OPERATOR AND MAINTENANCE MAN

Figure 14-1

BIT SPECIFICATION RECOMMENDATIONS

BIT PARAMETERS TO BE SPECIFIED SHOULD BE CHOSEN FROM A
STANDARD LIST OF WELL-DEFINED PARAMETERS WHICH HAVE WELL-
DEFINED VERIFICATION METHODS

NUMERICAL BIT REQUIREMENTS MUST BE DERIVED FROM OPERATIONAL
AND LOGISTIC REQUIREMENTS THROUGH TRADE-OFF ANALYSIS

SPECIFICATIONS FOR MULTIPLE-APPLICATION SUBSYSTEMS MUST
BE BASED UPON WORSE CASE HISTORICAL/PREDICTED OPERATIONAL
AND LOGISTIC REQUIREMENTS

DRAFT RFPs MAY BE USED TO OBTAIN FEEDBACK ON REASONABLENESS
OF REQUIREMENTS

ALL FAILURES MUST BE ACCOUNTED FOR, TRADING OFF AUTOMATIC/
MANUAL TEST, BIT/ATE, ETC.

Figure 14-2

BIT EVALUATION RECOMMENDATIONS

HOLD BIT DESIGN REVIEWS. REQUIRE BIT ANALYSIS EARLY ENOUGH TO IMPACT SYSTEM DESIGN. REQUIRE FAVORABLE BIT PREDICTIONS BEFORE PROCEEDING WITH DEVELOPMENT.

USE BIT AND TECHNICAL MANUALS AS PART OF FACTORY ACCEPTANCE AND IN TEST AND EVALUATION.

DEMONSTRATE BIT USING MIL-STD 471 PLUS . . .

MAKE EXTENSIVE USE OF INSTRUMENTATION TO PERMIT CHARACTERIZATION OF FAILURES

ESTABLISH A CLOSED LOOP DATA SYSTEM TO MEASURE BIT EFFECTIVENESS.

Figure 14-3

BIT MANAGEMENT RECOMMENDATIONS

REQUIRE AN INTEGRATED DISGNOSTIC PROGRAM
CONSIDER DIAGNOSTICS AS A SYSTEMS ENGINEERING DISCIPLINE
DEVELOP DISGNOSTIC IN PARALLEL WITH HARDWARE
EMPHASIZE VERTICAL TESTABILITY

PROVIDE PROPER VISIBILITY AND FUNDING EARLY IN DEVELOPMENT

ESTABLISH CORPORATE MEMORY
CENTRAL REPOSITORY (TECHNIQUES/PERFORMANCE/COST DATA)
LESSONS LEARNED
SINGLE POINT OF CONTACT
DEFINE BIT "COMMUNITY"
ESTABLISH STANDARD TERMINOLOGY
PROVIDE EDUCATION FOR MANAGERS

Figure 14-4

BIT WORKSHOP PANEL NO. 3 REPORT:
SYSTEM BIT

PANEL CHAIRMAN: CAPTAIN DAN GLEASON, RADC

Captain Gleason is the
Maintainability Design
Engineer for the RADC

HIGHLIGHTS OF THE PANEL REPORT

Issues and observations addressed by the System BIT panel are shown in Figure 15-1, through the various phases of system acquisition. Certain definitional problems exist (e.g., false alarms) that should be addressed. One hundred percent diagnostics are essential for a successful system. A "thread" tracing CNDs and RTOKs into the field via a closed loop data collection system may be required in order to determine the causes for system deficiencies.

The sequence of issues is shown in Figure 15-2. The final issue is that of communicating user needs to the system developer and the system contractor. The consensus was that the using command must be in at the beginning of the process presenting a "wish list" of requirements to the system developer that may or may not be achievable in terms of such requirements as turnaround time, sortie generation and other numbers of that nature. The process of communicating these requirements from the using command to the system developer may be assisted by a system evaluator (e.g., Army, SEG: Air Force, AFTEC). This type of system evaluator deals with fault detection and fault isolation problems as related to user requirements such as turnaround time. As such, the system evaluator would act as an interpreter between the "wish list" of the user and the procurer's specification requirements. A great deal of interaction between user groups, system developers, and system contractors is essential to this process. Realistic and stringent contractual specifications in terms of MTTR,

M_{MAX} , reliability and availability requirements are needed to establish the basic reliability and maintainability characteristics of the system, within the constraints of the support requirements.

Support requirements demand a 100 percent diagnostic capability (automatic and/or manual) to be achieved with specified maintenance skill levels. Nonaddressable failures cannot be permitted since they drive MTTR excessively high. Systems that specify percentages of automatic FD/FI (e.g., 90 percent) to the contractor result in his concentrating on this 90 percent and neglecting the other 10 percent to the detriment of overall maintainability (e.g., support, training, etc.). In some cases, only 80 percent automatic FD/FI is achieved; when this occurs, the 10 percent shortcomings (between 80 and 90 percent) has not been planned for support equipment. The turnaround (when the automated BIT did not work) presents extremely difficult maintenance problems.

Attempts to translate requirements such as maintenance personnel skill levels to system maintainability requirements thus far have proved to be relatively unsuccessful. It does not appear that industry has the expertise to perform such a translation. This may be a worthwhile area for investigation.

Limitations should be placed on the quantities of spares available and the number of removals permitted in order to prevent indiscriminate replacing of boxes to meet specified MTTR requirements.

Limits on CNDs and RTOKs should be considered as possible specification characteristics to be measured under certain specified and controlled conditions.

Contractual incentives should be considered such as Maintainability Improvement Warranties (MIW) comparable to RIWs,

using thresholds and goals as well as maintainability improvement growth.

Figure 15-3 indicates the requirements of system contractor management including converting general requirements into specific requirements, performing tradeoffs, and subcontractor management. This approach gives the contractor the flexibility required to optimize the diagnostic function. The "hard" requirement should be MTTR with the contractor determining the FD and FI percentages and the automatic/manual breakdown. In all cases, the overall diagnostic system must provide 100 percent FD and 100 percent FI.

In addition to the characteristics shown, "Vertical Testability" (capability of O, I, and D-level testing) is a system requirement.

Subcontractor management does not appear to be a difficult problem, provided the listed tasks are performed. High level summaries may consist of data such as percentages of various functions covered by BIT, as opposed to analyses such as FMEAs.

Figure 15-4 indicates items required during system contractual validation. Continued monitoring and evaluation from the beginning are required to assess system maintainability.

The possibility of making the maintainability demonstration of MIL-STD-471 more realistic by combining it with some environmental tests should be considered.

DISCUSSION POINTS

- The "smart box," "dumb man" concept apparently offered by the extensive use of BIT is not a viable concept since highly skilled maintenance personnel are required for the "beyond BIT" maintenance problems. Technicians capable of independent diagnosis of the system faults are still required, regardless of the sophistication of the BIT.

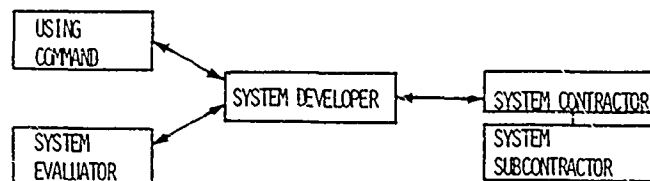
- The number of highly skilled technicians versus the number of low skill level technicians is a problem to be addressed relative to the BIT capabilities of the system. It has been mistakenly assumed in many cases that no highly skilled technicians ("smart guy") are required because of the capabilities provided by the BIT.
- "Management" of a program seems to end at the end of development and no suitable vehicle presently exists to adjust changed system maintainability characteristics to the production system.
- As BIT gets better and better, the personnel skill level problem is aggravated because the requirement for a skilled maintenance man still exists and because it is easier to manage a maintenance staff with a 6 to 1 unskilled to skilled ratio than it is a 100 to 1 ratio staff. In addition, it is more difficult to maintain high skill levels because fewer problems are seen.
- Developing the training for the second level of support (comparable to I-level) in the commercial industry is more difficult than for the first level (comparable to 0-level); therefore, it is done first.
- The CND rate is approximately 30 percent in the military, in industry, and the airlines, whether fault detection is done automatically or manually.
- BIT has to be "tailored" to the type of system in which it is incorporated to adapt it to the specific constraints on the system.
- MTTR should be considered for being specified as two values, one in the manual and one in the automatic mode, identifying the percent of time it is performed in each mode. Constituents of the MTTR should be considered for specifications to address the problem of high-time contributors to total MTTR.
- MTTR requirements must be related to support costs so that reductions in MTTR do not result in excessive support costs.
- BIT must be used in the way it was planned for use in order to realize its full benefits.
- In view of the fact that two to three years are required in operational use to mature the BIT, it is not possible to provide hard numeric values early in the program to determine that contract requirements and user constraints have been met. This makes it difficult to meet DSARC requirements for such values.

- Funding and personnel are required to identify BIT problems and to implement solutions during the two to three year BIT maturing period.
- More BIT cleanup could be performed during the system development phase if more attention were given to this aspect of the system, including participation by users. This requires early management and design attention applied to the problem.
- BIT design flexibility permitting changes to be implemented by software can decrease the amount of time required to mature the BIT, possibly permitting a one-year maturing period instead of the current two to three year period.

ISSUES/OBSERVATIONS

1. BIT FIELD PERFORMANCE LESS THAN SPECIFIED AND DEMONSTRATED.
2. CURRENT APPROACHES DO NOT TAKE INTO ACCOUNT FALSE ALARMS UNDETECTED FAILURE, RETOK, CND.
3. BIT PERFORMANCE NOT COMPATIBLE WITH MANPOWER AND LOGISTICS REQUIREMENTS.
4. INADEQUATE RESOURCE AND SCHEDULE ALLOCATION.

Figure 15-1



SYSTEM CONTRACTUAL SPECIFICATIONS STRINGENT REALISTIC GENERAL SPECIFICATIONS

1. PERFORMANCE REQUIREMENT
 - MTTR, Max
 - MTBF
 - AVAILABILITY
2. SUPPORT REQUIREMENTS
 - 100% DIAGNOSTIC CAPABILITY
 - MAINTENANCE SKILL LEVELS
 - SPARES LIMITATIONS (MTBR)
 - CND, RETOK LIMITS
3. CONTRACTUAL INCENTIVES
 - WARRANTIES
 - THRESHOLD: GOALS
 - GROWTH

SYSTEM CONTRACTOR MANAGEMENT Figure 15-3

CONVERT GENERAL REQUIREMENTS INTO SPECIFIC REQUIREMENTS

- FD/FI
- AUTOMATIC
- MANUAL

PERFORM TRADEOFFS

- BIT ARCHITECTURE
- BIT TECHNOLOGY
- OFF THE SHELF VS. NEW DESIGN
- MAINTENANCE VS. OPERATOR BIT
- INCORPORATE BIT DATA INTO I-LEVEL TESTING

SUBCONTRACTOR MANAGEMENT

- ALLOCATE SPECIFIC REQUIREMENTS
- COMMUNICATE SYSTEM DESIGN APPROACH
- DATA REQUIREMENT
 - SYSTEM CONTRACTOR
 - TEST STRUCTURED FMEA
 - BIT ACCURACY
 - TOLERANCE LEVELS
 - TEST POINT SELECTION
 - SYSTEM DEVELOPER
 - HIGH LEVEL SUMMARY - REGULAR BASIS
 - DETAILED LEVEL - AVAILABLE ON REQUEST

SYSTEM CONTRACTUAL VALIDATION

Figure 15-4

- DEVELOPMENT OF TEST FACILITIES & HARDWARE
- CONTINUAL EVALUATION & MILESTONES (TAAF)
- REALISTIC M-DEMO
- COMBINED ENVIRONMENTAL TESTING
- SIMULATE OPERATIONAL ENVIRONMENT
 - MANPOWER
 - T.O.s
- OPERATIONAL EVALUATION
 - SYSTEM SHAKEDOWN
 - FALSE ALARMS, CNDS
 - UNANTICIPATED OPERATIONAL ENVIRONMENTS
 - UNANTICIPATED FAILURE MODES
 - EVALUATE PERFORMANCE REQUIREMENTS
 - EVALUATE SUPPORT REQUIREMENTS

APPENDIX A

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